FabTime Cycle Time Management Newsletter

Volume 5, No. 2 February 2004

Information

Mission: To discuss issues relating to proactive wafer fab cycle time management

Publisher: FabTime Inc. FabTime sells cycle time management software for wafer fab managers. New features in the current version (6.0) include the ability to filter and slice by tool model and vendor on tool analysis charts.

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Welcome

Welcome to Volume 5, Number 2 of the FabTime Cycle Time Management Newsletter. We have a big jump in subscribers this month, thanks largely to a series of cycle time management courses that we held at Analog Devices in Limerick, Ireland. Analog Devices is now third in terms of number of subscribers (jumping into the top ten list for the first time). And, in something of a personal milestone for me, the subscriber list has just passed 1500. A special welcome to all of you new subscribers!

Community announcements for this month include notices for two presentations that I'll be making at APICS meetings, in Fremont and Ventura, California. Subscriber discussion topics for this month include nine responses to last month's topic of Cycle Time and Yield. These responses point out some significant omissions in our article. Therefore, instead of introducing a new main article, we've chosen to revisit the topic of cycle time and yield, and very briefly summarize the additional points made by contributing subscribers. We will have a new topic next month, and we thank the subscribers who took the time to contribute.

Thanks for reading!—Jennifer

FabTime

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Community News/Announcements

FabTime APICS Presentations in Fremont and Ventura, CA

FabTime's Jennifer Robinson will be giving a Keynote Presentation on Current Issues in Cycle Time Management at the March 3rd meeting of the APICS Mission Peak Chapter in Fremont, CA. The abstract is included below. The meeting will be at 7 pm, at Massimo's Restaurant in Fremont. The cost to attend (including the presentation and dinner) is $23 for students, $28 for APICS members, and $35 for non-members. RSVP to Ann Ibach at 510-494-9531 or ann_ibach@hotmail.com. Attendance is first-come first-served, and non-members are welcome to attend.

Jennifer will also be speaking on cycle time management on March 9th, at the APICS Ventura Chapter in Ventura, CA. That meeting will be held at 6 pm (dinner at 6:30, presentation at 7:45), at the Amgen Conference Center. The cost is $15 per person (including the presentation and dinner), and you may register online at http://www.apics-vc.org/.

Abstract:
This talk focuses on cycle time-related issues for manufacturing facilities. Topics discussed include benefits and challenges of cycle time management, the relationship between cycle time and utilization, the cycle time impact of downtime and variability, useful metrics for improving cycle time, and the top cycle time issues observed today in manufacturing. The talk emphasizes the fundamental relationships underlying factory behavior, and uses concrete examples to illustrate how operational decisions can affect cycle time. Although the speaker's background has primarily included work with semiconductor factories, the talk is designed to be of general interest to people from all types of manufacturing facilities.

FabTime welcomes the opportunity to publish community announcements. Send them to newsletter@FabTime.com.

FabTime User Tip of the Month

Login Page and Home Page Bulletins

You may have noticed time-sensitive messages on the FabTime login page at your site, or on your home page, about system updates, etc. What you may not know is that any user with permission to do so can create these types of messages. These permissions are disabled by default, but if you have a need to share messages with other FabTime users at your site, you can ask your system administrator to give you bulletin board permission. Bulletin board messages can be created on the home pages of individual users (e.g. for people who report to you) or can be displayed for all users (on the login page or on all of the home pages). Possible examples might include:

- Planned shutdown of the MES for system upgrades.
- Short-term focus on lots of particular product type.
- A new super-hot lot that's being started today, to which everyone should give special attention.

- Short-term focus on a particular tool that's experiencing problems (for a specific set of users).
- Pager or cell phone contact information for technical support.

Once you have permission to create bulletin board messages, click on the "Manage FabTime Bulletins" link (available on your home page and on the chart list page) to get to the bulletins user interface. Here you can create new bulletins, or edit or delete bulletins that you've already created. Click on the link to "add a new bulletin board message" to get started. You'll need to specify a start time (defaults to now), an end time (defaults to 24 hours from now), and a brief message. You use check-boxes to indicate whether the message should be displayed on the FabTime login page, all home pages, or specified user home pages. You then select any specified users from drop-down lists (if the message is not global), and click the "save" button. Your bulletin board message will be created, and will start being displayed as soon as the start time is passed (usually immediately).

If you have any questions about this feature (or any other software-related issues), just use the Feedback form in the software.

Subscriber Discussion Forum

Issue 5.01 – Cycle Time and Line Yield

Mike Hillis wrote "Some thoughts on the cycle time:die yield discussion... I believe there is indeed a relationship between cycle time and die yield. However, my sense is that the relationship is more based on cycles of learning rather than baseline defect density or other physical risk.

Modern fabs are pretty clean places. I would suggest that the overall fab environment has less to do with defect density than tool excursions. These tend to be "event" based and the age of the lot has nothing to do with it being at a particular tool when it fails. Obviously, it's best to find that out as soon as possible so that the problem can be resolved. Hopefully, such excursions will be caught by in-line inspection or metrology.

This is not to suggest that there is no cycle time impact on yield improvement, however. In these days of short product lifetimes, rapid technology ramps and cost control, it is essential that fab and product engineers get rapid and meaningful feedback on the fab's performance. Squeezing the last bit of yield out of each wafer depends on continuous improvement. Expediting experimental or "soft start" lots will give the engineer an opportunity to quickly determine the value of a change he or she may wish to make. However, the real test comes in volume production. Brisk cycle times on "standard" priority material ensure that

changes are efficacious in volume.

The successful and rapid introduction of new technologies is clearly impacted by cycle times. Product, Integration and Fab engineers all require timely feedback to meet technology roadmap requirements. The yield learning curve is dependant on figuring out what went wrong and then making changes to correct previous assumptions. Long cycle times lead to flat learning curves, clearly an undesirable circumstance.

It is my thought that these cycles of learning have a much greater impact on yields than incidental defectivity. Once in the sweet spot (mature yields, process, etc.) cycle time becomes more of a WIP management (Manufacturing and Planning) concern than one of yield management. The key is to get to that point as rapidly as possible. Older fabs that are pushing the limit on technology might be more sensitive to the cycle time:yield relationship due to environment. Perhaps this discussion has merit in that arena."

Ellis Errett, Ph.D. (Sandia National Laboratories) wrote: "After reading your article on cycle time and Yield, I could not keep my thoughts to myself. I have been in wafer fabrication for most of 35 years, many of which were in small volume, development fabs. One major deviation that I took from wafer fabrication was 5 years spent in the employment of the Thomas Group. Our philosophy and mode of operation at the Thomas Group fit very well with my previous 20 years of experience in the semiconductor industry. Short cycle time has a beneficial effect in multiple aspects of any business. Since I had been a wafer fab engineer and manager for many years, it was easy for me to set up cycle time measurement systems in fab operations and track the benefits of short cycle time.

The Key component that was not mentioned in your article is Cycles of Learning. Especially in the technology development phase or beginning of a production phase, cycles of learning are very important. Feedback from each lot is necessary to make adjustments in processes and procedures. If feedback from a low volume development line occurs once in 10 weeks, progress will be slow. Higher volume may help if there is sufficient capacity to keep the cycle time low. Feedback every 3 to 5 weeks will lead to successful development much quicker. The same is true for yield. A major component in yield in an immature production line is Systematic Yield limiters. Systematic defects are created by process marginalities that can drive yield to zero very quickly. Short cycle time and hence increased cycles of learning will eradicate systematic defect modes quickly.

I do not have specific numbers on any of the yield improvements that I have observed during my time in wafer fab operations. However, I have seen many times, the positive effect on yield through increased cycles of learning due to short cycle time.

In an additional note, I have observed numerous times the classic situation of a failure in line that goes undetected until first electrical test. With long cycle time, many wafers are at risk of being scrapped, but with short cycle time the risk is much less. (Risk is reduced with a shorter cycle of learning)."

Frans Brouwers (Philips Semiconductors) wrote: "I would like add some remarks on the discussion on yield gain.

1. The impact of Time Criticals

We all have Time Critical Sequences in our fab. We all have learned to manage them. It might be the case that we succeed very well in that. And this leads to a situation were yield and cycle time do not relate any more. We simply have scheduled the relationship out of our fab.

As a result, yield impact prevention has an impact on capacity.

2. The impact of short quality feedback loops

Short cycle times create a short feedback loop on quality incidents. This gives you the opportunity to shut down tools creating quality losses. If your quality control system focuses on early warnings and preventive shutdowns, the yield impact will be minimal. Again this will lead to the situation where we have managed to reduce the yield impact.

3. The impact of (yield) improvement projects

In my view the big gain of short cycle time is in this field. Short cycle time leads to:

- Short feedback loops, resulting in early warnings, resulting in starting improvement projects
- Short cycle time of experiments leads to a faster improvement rate, leading to a higher yield.

Although I have no data to back this belief, from my experience I know this to be true. But it should be possible to get evidence from Sematech: fabs with shorter cycle time should have a higher yield improvement rate.

4. The impact of management policy making

Yield as well as cycle time is subject to management policy making "how much yield losses are acceptable in our business". The acceptability is a function of:

- Marketing your fab as a quality fab
- The need for fast ramp-up
- The cost of yield

So, in summary, I believe that you will not find a relation between the cycle time and yields of individual lots. If there is a relationship, it can be found in the improvement rates of especially new processes."

Dan Siems of Philips Semiconductor wrote: "I would like to echo what Frans is saying --- cycle time impacts the yield learning rate. This data can be 'gotten' ---- most fabs will show their yield learning curves (normalized) and cycle time statistics, but is difficult. However, we can look at it another way. The amount of time a wafer spends in the fab does not really open it up to more random defect possibilities ---- what really happens is that this wafer has too much 'old process' built into it compared to its companion wafers of the same vintage. A wafer fab is constantly in flux, hopefully biased toward improvement. Wafers that stay in the line longer because they travel more slowly than other wafers have not had incorporated into them the latest 'fixes' from earlier process steps that wafers traveling faster -- but coming out at the same time -- have gotten. So they have poorer yields."

David Trestain of WaferTech wrote: "Regarding yield vs. cycle time, one other influence which I believe is highly important but is missing from your discussion is the other main reason for cycle time variability for different lots (especially in a stable line) – the hold rate.

Many lots with long cycle time have invariably been on hold for trouble dispositions of any sort – from as simple as SPC rules violation, which require resampling, to defectivity alarms from inspection, reworks, tool aborts, etc. Each event adds age to the specific lots involved, and by the very nature of being caught in a "problem" event, they will have captured the most variation of all lots in the line. Variation, most device engineers will support, will lower the yield as the device will be out of the "sweet spot", especially if the design or process doesn't have much margin.

It has been interesting to plot yield vs. hold count per lot, as well as "hold hours" vs. yield, as opposed to just total cycle time or queue time. You need to exclude engineering lots and their "hold hours" as they are added for a very different reason."

Bernhard Renelt (Infineon Technologies) wrote: "Thanks for opening the discussion topic "interaction between cycle time and yield" in the last FabTime issue. As you already mentioned in your statement, everybody expects a relationship between cycle time and yield in that way, that long cycle time causes lower yield. But I would like you to think also of the opposite case: low yield lots cause longer cycle times.

Please assume the following situation: A lot is facing a problem during processing, which might be the cause for yield loss. The lot is set on "Hold". A process engineer has a closer look at this lot, does some additional measurements. Finally the lot will see some rework steps and will set again on its production route. The whole procedure takes 5 days cycle time. In this case the yield (process problem) is the cause of longer cycle time, not the effect."

Laura McClure (IBM) wrote: "I just read your most recent newsletter and found the topic interesting. One thing that stuck out to me is that there was no mention of the impact of faster cycle time on yield learning and process centering. The FabTime article referred to the benefits of reduce cycle time as "The less time wafers spend in the fab, the less opportunity they will have to be contaminated or damaged". I think most would agree that additional benefits are found in reduced "mean time to detect" and shorter in-line metrics feedback loops."

Madhav Kidambi (Infineon Technologies) wrote: "We have changed the dispatching rule in our fab and we measured the cycle time before and after the implementation of dispatching rule. We did find a significant reduction in standard deviation of cycle time. Also we compared the yield before and after the implementation of dispatching rule and the data showed that the lower the cycle time the better the yield. We also found that the standard deviation of yield was much tighter after we implemented the dispatching rule. But here is the catch: it is really hard to quantify or accept the data as many changes are made to the process to improve yields, and it is an ongoing process. So it is hard to correlate the cycle time and yield. Our site statistician said that it is hard to prove it statistically because of the nature of the data. So I would be very much interested if anyone can form a method which can correlate the cycle time and yield based on the historical data. The only way we see it is to design an experiment with 25 lots or so and run them through the line through the same process conditions and then quantify. This seems to be a difficult task because of the length of the cycle times."

Philippe Vialletelle of ST wrote: "From my point of view, there is no straight correlation between the cycle time of one individual lot and its final yield. It's much more a matter of operating strategy of the fab and of global influence on the way in which yield is managed.

- Longer cycle times usually come from higher utilization of equipment. Consciously or not, engineers may be pushed by management directions to get to less severe levels of "triggering" for out of control action plans or maintenance. They can tolerate slight degradations of process "quality", not important when taken individually, but that may jeopardize product yield when combined all together.

- Longer cycle times also mean more wip in the line on one hand and more time to get the yield alert if the problem is detected at parametric testing! That's to say more wafers scrapped hence lower yield. Shortest cycle times mean shortest reaction loops and less wip impacted by defect."

Cycle Time and Yield Revisited

Introduction

When we wrote about cycle time and yield last month, what we said, in summary, was "We think it likely that reducing cycle time will improve yields. The less time wafers spend in the fab, the less opportunity they will have to be contaminated or damaged. Scrapping wafers also increases variability in the fab, which increases cycle time." Well, after reading the subscriber feedback above, we still think that reducing cycle time will likely improve yields. But we've become convinced from the discussion above that the primary reason for this improvement has more to do with increased cycles of learning than with exposure to contamination.

We also believe that the relationship between cycle time and yield is much more circular than we had previously described. If you improve yields, you will likely reduce variability in your line. Which will tend to improve cycle time. You will also be able to start fewer wafers, which will increase standby time on your critical tools, and improve cycle time. But improving cycle time will also tend to improve yields, for all of the reasons described above. So, you may have a positive interaction cycle between the two. Of course, this is not guaranteed. One way to improve yields is to do more testing, which will increase cycle time (directly through the tests and through increased equipment utilization). And one way to improve cycle time is to rush lots through the fab, without any testing, at the obvious expense of the yield. So, it's not necessarily straightforward, and a balance between cycle time and yield goals is necessary.

However, we do have a short list of conclusions that we have summarized from our previous article, and from the subscriber contributions above.

- There may or may not be a relationship between the cycle time and yield of individual lots. Even if there is, it will tend to be very difficult to quantify, because of the variability in the fab and the length of the average cycle time. Even if there isn't a direct relationship for individual lots, there are some generally positive trends related to cycle time and yield, listed below.

- Shorter cycle time leads to increased cycles of learning, and faster yield ramp.

- Shorter cycle time may result in less opportunity for contamination, and hence higher die-per-wafer yields.

- Shorter cycle times can lead to quicker identification of yield problems, through shorter "mean time to detect" errors, and shorter in-line feedback loops.

- Non-engineering lots that spend significant time on hold will tend to have longer cycle times (because of the hold time) and worse yields (because the holds are often because of problems to begin with) than other lots. In this case it's more that the yield problem causes the cycle time problem (through hold and rework time) than vice versa.

Summary

The relationship between cycle time and yield is complex, and involves management trade-offs related to equipment utilization and amount of in-line testing. In general we, and many of the people we've talked with, believe that some relationship does exist. We think that improving cycle time will tend to improve yields, and vice versa. This improvement may not be visible or quantifiable at the individual lot level, but will likely show itself through cycles of learning and improved yield ramp times.

We would like to conclude by thanking the subscribers who took time to share their knowledge on this topic. You've greatly improved our understanding regarding cycle time and yield, and dramatically improved the quality of this discussion in the newsletter.

Subscriber List

Total number of subscribers: 1505, from 374 companies and universities. 26 consultants.

Top 10 subscribing companies:

- Intel Corporation (69)
- Motorola Corporation (57)
- Analog Devices (50)
- Infineon Technologies (47)
- Philips (45)
- STMicroelectronics (45)
- Seagate Technology (42)
- Micron Technology, Inc. (40)
- Texas Instruments (37)
- Advanced Micro Devices (36)

Top 3 subscribing universities:

- Arizona State University (12)
- Technical University of Eindhoven (7)
- Virginia Tech (7)

New companies and universities this month:

- Crystal Technology
- ILOG
- Rutgers University
- ST Assembly Test Services

Note: Inclusion in the subscriber profile for this newsletter indicates an interest, on the part of individual subscribers, in cycle time management. It does not imply any endorsement of FabTime or its products by any individual or his or her company.

There is no charge to subscribe and receive the current issue of the newsletter each month. Past issues of the newsletter are available for a small fee from FabTime's Amazon zShop, at www.amazon.com/shops/fabtime.

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FabTime® Cycle Time Management Training

"It was helpful to see best-in-class methods for wafer fab cycle time management. Discussing these matters in-depth with you was quite valuable, as we could ask questions specific to our fab and processes."

Shinya Morishita
Manager, Wafer Engineering
TDK Corporation

Course Code: FT105

This course provides production personnel with the tools needed to manage cycle times. It covers:

- Cycle time relationships
- Metrics and goals
- Cycle time intuition

Price

$4950 plus travel expenses. On-site delivery for up to 15 participants, each additional participant $195. Discounts available for multiple sessions.

Interested?

Contact FabTime for a quote.

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Web: www.FabTime.com

Do you make the best possible decisions?

- Do your supervisors possess good cycle time intuition?
- Are you using metrics that identify cycle time problems early?
- Can you make operational changes to improve cycle time?

FabTime's Cycle Time Management Training is a one-day course designed to provide production personnel with an in-depth understanding of the issues that cause cycle time problems in a fab, and to suggest approaches for improving cycle times. A two-day version is also available upon request.

Prerequisites

Basic Excel skills for samples and exercises.

Who Can Benefit

This course is designed for production personnel such as production managers, module managers, shift supervisors, hot lot coordinators, and production control.

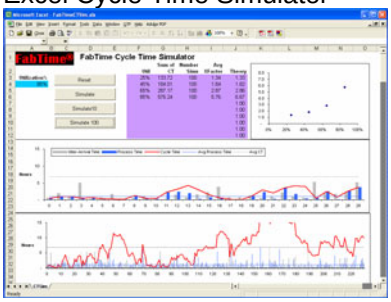
Skills Gained

Upon completion of this course, you will be able to:

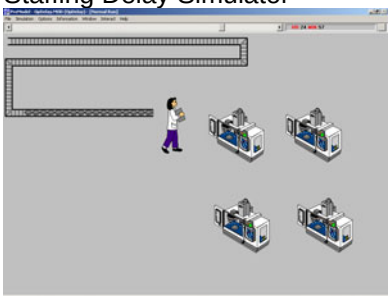
- Identify appropriate cycle time management styles.
- Teach others about utilization and cycle time relationships.
- Define and calculate relevant metrics for cycle time.
- Teach others about Little's law and variability.
- Quantify the impact of single-path tools and hot lots.
- Apply cycle time intuition to operational decisions.

Sample Course Tools

Excel Cycle Time Simulator



Staffing Delay Simulator



Additional Half-Day Modules

- Executive Management Session.
- Site-Specific Metrics Review.
- Capacity Planning Review and Benchmark.