# FabTime Cycle Time Management Newsletter

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## Information

**Mission:** To discuss issues relating to proactive wafer fab cycle time management.

**Publisher:** FabTime Inc. FabTime sells cycle time management software for wafer fab managers.

**Editor:** Jennifer Robinson

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## Welcome

Welcome to the second issue of FabTime's Cycle Time Management Newsletter! The big news this month is that the number of subscribers has almost tripled, from 33 for the first issue to 93 for this issue. Many thanks to all of you who helped by forwarding the newsletter to your colleagues!

The Cycle Time Management newsletter is a free publication, distributed monthly by email. If you know of anyone who you think would like to participate, please forward them a copy of the newsletter, and then ask them to email Jennifer.Robinson@FabTime.com to subscribe.

In this second issue, the theme is the P-K formula, the mathematical justification for variability reduction efforts in a wafer fab. We welcome suggestions for future newsletter themes, and contributions in the way of news, questions, book recommendations, etc. We don't want the newsletter just to be about us, FabTime, we want it to be about the community of people interested in this area, and the work that we all are doing. Thanks for participating!

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# Definition of the Month

## The P-K Formula - The relationship between WIP, utilization and service time variability

The Pollaczek-Khintchine (called P-K, for obvious reasons) formula gives the expected average WIP at a single-tool workstation where arrivals to the workstation are highly variable, and process times are somewhat less variable. More specifically, the formula applies when interarrival times to the workstation are exponentially distributed, and process times follow a general distribution (what is known as an M/G/1 queue). For tools that fit this description, the expected WIP can be easily computed from the mean interarrival time, the mean process time, and the variance of the process time distribution.

It turns out that in a wafer fab, interarrival times to a given workstation usually are highly variable, and some research suggests modeling them as exponential. We usually think of process times as being fairly constant. However, you can look at total process time from the lot's perspective as the time from when a lot gets to the front of the queue to when it finishes processing. In this case things like setups, equipment downtimes, operator delays, and different operations processed on the same tool all add variability to the process times seen by successive lots. And this variability, as shown by the P-K formula below, can drive up WIP.

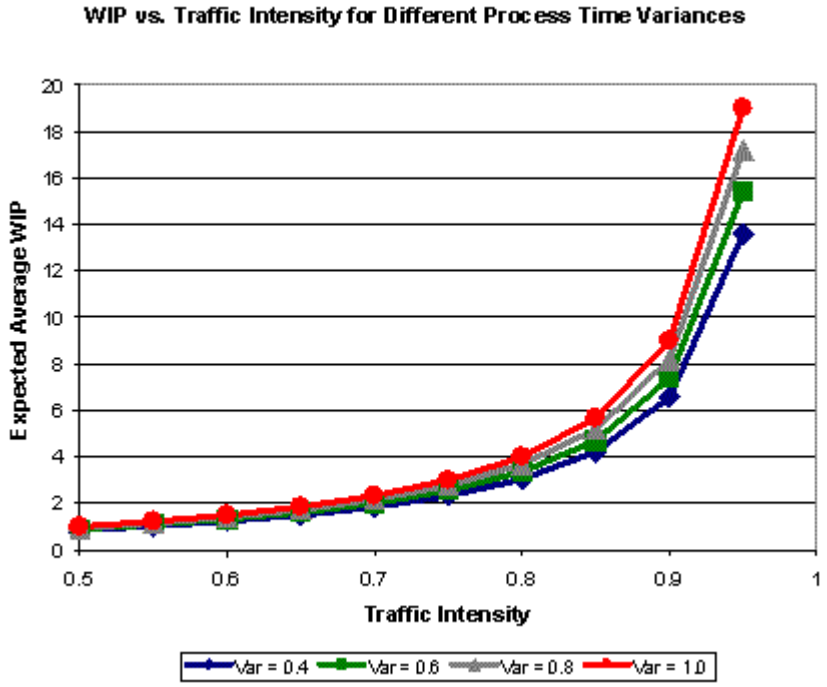
- WIP = average number in queue and in process (units)
- $\lambda$ = arrival rate (units per hour)
- $\mu$ = service rate (units per hour)
- $\rho$ = lambda/mu (traffic intensity or loading)
- $\sigma^2$ = variance of service time distribution (0 for constant service times, 1 for highly variable service times)
- $WIP = \{\rho\} + \{[\rho^2]/[2*(1 - \rho)]\} + \{[\lambda^2*\sigma^2]/[2*(1 - \rho)]\}$

If you look at the above formula for WIP, you see that it is first of all a function of traffic intensity (in this simple case, traffic intensity is the same as equipment loading). We know this. As a tool is loaded more heavily, the number of wafers in the queue increases. As rho approaches one, the denominator of the last two terms approaches zero, and the WIP approaches infinity. This is why capacity planners always plan for a capacity buffer on each tool group - to keep the WIP from becoming very large. You'll also notice in the P-K formula as I've stated it above, that the last two terms in curly brackets have the same denominator, and could be combined. I separated them to highlight the influence of process time variability. If you have constant process times, the whole last term drops off. If you have highly variable process times, that term can become significant. A graph illustrating this is included on the following page.

The graph shows that it is largely equipment loading that drives cycle time at individual tools (we're implicitly accounting for the downtimes, etc., in the service time variability). If we just care about reducing cycle time, we can decrease start rates or increase capacity, and cycle times will go down. However, either of these approaches costs money. The nice thing about variability reduction is that it also reduces cycle time, without requiring costly equipment purchases or decreased start rates.

This example is clearly a simplification of the situation in a wafer fab, but the concept holds true. The P-K formula tells us that, if we look at individual tools in the

fab, anything that we can do to reduce variability in the process times seen by successive lots will directly act to reduce WIP at these tools, without requiring a reduction in tool loading. And, as will be discussed in the next issue of the newsletter, cycle time will go down at the same time. The P-K formula is the mathematical justification for variability reduction efforts in a wafer fab.




## Discussion Question Responses

Last month's question was "what do you think is the biggest source of variability in a wafer fab?" Several people took the time to send in their thoughts on this subject, and I have included these responses below.

### John Fowler (ASU)

"Operator/technician availability and Skill levels."

### Bob Kotcher (Headway)

"We are a small read-write head fab with heavy R&D usage of the fab (one common fab for both production and R&D). In answer to your question about our biggest cause of variability here, I'd say it's tool downs. Our uptimes are good, but, being a small fab, we have several tool groups that consist of only two tools. Such tool groups that are loaded more than 50% of capacity (most of them) see queues grow quickly whenever one of the tools is down for any length of time (because capacity loading on the remaining tool becomes >100%)."

### V.A. Ames (Applied Materials)

"I believe that equipment variability is the biggest contributor to high cycle times. Of the factors that Jennifer mentions in her question, batching, setups, equipment failures, rework, and scrap could (and usually do) involve equipment variability.

Another major factor leading to high cycle times not mentioned is operator and equipment support skill levels. Toyota understood this 30 years ago when they introduced TQM and JIT into production. If the basic equipment conditions vary, then quality will vary. If equipment down-time varies, then JIT is very difficult, if not impossible, to implement. This is the reason they created Total Productive Maintenance (TPM), to reduce equipment variability. It has proven to reduce set up time, eliminate most equipment related failures and quality issues, and because one of its key components is focusing on operator and maintenance support skills, turnover and cross-training do not impact cycle time. Several US semiconductor companies have finally come to understand this and are implementing TPM in their fabs. The typical thought that equipment should just run everyday, with operators loading and unloading, maintenance completing PMs as the equipment manufacturer recommends, and fixing problems when the machine breaks will be coming to an end. It may take ten years, but as production facilities strive to compete in costs and cycle time, the attitude about how equipment is run and maintained will change. This applies to the equipment suppliers as well as the users.

The impact of equipment variability on cycle time depends on the number of bottlenecks and near constraints in the line. An R&D factory may have numerous bottlenecks due to the various lot releases, part numbers, and lot sizes. They usually have an advantage over large logic fabs, though, because the amount of product in the line is typically much less and cycle time requirements are not quite as stringent. The DRAM fab should have the least amount of impact from variability. The bottleneck is easier to define, and process changes (due to different part numbers) are less. Therefore, I would rate the impact of variability (as it should be) on the three types of fabs mentioned as: Logic - highest, R&D - in the middle, and DRAM - least impact."

### Stuart Carr (Consultant)

"In the question about what contributes most to variability, I thought I'd add another factor to your list there. That factor is high utilization: running one or more machines at or near "capacity" (even if only periodically, which relates back to other factors, like batching) greatly increases queueing delays, which increases variability and average cycle times. In other words, one can think of capacity as a buffer against the other sources of variability you listed, like breakdowns, batching, etc. By adding some "surplus" capacity, the effects of these (largely uncontrollable) sources of variability can be mitigated. (Of course, simulation or other analysis can be used to quantify the capacity/cycle time trade off.)"

### FabTime Response

I think that all of the things discussed above are correct, in that they are major sources of variability in wafer fabs. If you consider them in light of the discussion of the P-K formula (and the graph shown on our website), you'll see that John and Bob have both highlighted specific things that contribute to variability in process times from lot to lot, while V.A. has discussed equipment variability, and its relationship to equipment loading. Stuart correctly points out that my original list neglected the fundamental factor of equipment loading itself. When the equipment has plenty of "surplus" capacity, cycle time is not usually a problem at all.

My personal opinion is that batching is also a big contributor to variability, because of the way that grouping and ungrouping of lots affects downstream variability. Batching can make the variability in lot

arrivals to a workstation worse than exponential. I have also seen many times what poor choice of batch loading rules can do to a simulation model. Of course, I might be biased, because my Master's thesis was on the topic of batching - it was the first attribute of semiconductor manufacturing that I really learned about.
In any case, the situation may be improving. In a May 2nd press release on the Semiconductor Business News website, I read that in an effort to reduce wafer cycle times, Applied Materials and Lucent announced a partnership to greatly expand the use of single-wafer processing tools in Lucent's next-generation frontend chip-making technologies, replacing typical batch furnaces. The press release noted that "During last month's Fourth Annual Fab Management Forum in Grenoble, France, Applied Materials managers argued that the use of single-wafer processing tools across an entire wafer fab would reduce work-in-progress (WIP) by 30%, lowering cost and speeding the time it takes to ship semiconductors to the marketplace." Of course, whether or not rapid-thermal-processing tools are robust enough to be used so extensively in production remains an open issue. But it would be great from a cycle time reduction perspective.

I would still be interested to hear from you about the sources of variability in your wafer fabs. John, Bob, Stuart, and V.A. were all brave enough to write in with their thoughts, and I hope that other people will, too. Being able to identify the primary variability-contributing culprits is the first step towards making improvements. Thanks for your input!

## New Discussion Question

What can be done to reduce variability in process times? (See above for an expanded definition of process time that includes all time from when a lot is ready to process to when it actually finishes processing.). Please send your input to Jennifer.Robinson@FabTime.com.

# Community News/Announcements

I was able to meet several newsletter subscribers for the first time at the Modeling and Analysis for Semiconductor Manufacturing (MASM 2000) conference in Tempe last week, as well as seeing many old friends from my SEMATECH days. The conference was very successful, and well-organized. There were more than 150 people pre-registered, and seemed to be about 200 in attendance. What made the conference nice, I thought, was that everyone there was interested in performance analysis for wafer fabs, and the attendance was small enough to make it very easy to meet people. I saw a number of interesting talks, and only regretted that sometimes the parallel tracks made it impossible to see everything that I was interested in. I recommend this conference to you for next year.

The MASM plenary talk, on the Competitive Semiconductor Manufacturing Survey's economic models for wafer fabs was especially interesting to those of us involved in cycle time management. The study's authors (Rob Leachman, John Plummer, and Nancy Sato-Misawa) suggest that revenue per yielded wafer declines 25% per year throughout the life of a process, suggesting a direct impact of cycle time on sales revenue. In one example that they gave, this works out to a cost of $3.04 per wafer incurred from a single day's delay, just because of cycle time. You can find the study's cost models at euler.berkeley.edu/esrc/csm.

While on the subject of conferences, Pres White of UVA made an announcement at the MASM conference asking people to mark the date for the 2000 Winter Simulation Conference. The conference will have a semiconductor manufacturing applications track again this year, coordinated by Tom Jefferson of Intel Corporation. I expect it to include a great set of papers related to simulation modeling for wafer fabs, and recommend that you attend if you can. Besides, this year's conference is in Orlando, and who can resist Disney World? The conference is scheduled for December 10-13, at the Orlando Wyndham Gardens. See www.wintersim.org for details.

FabTime welcomes the opportunity to publish similar announcements for other companies. Simply send them to Jennifer.Robinson@FabTime.com.

# FabTime Recommendations

- FabTime's book of the month for May is Microchip Fabrication, by Peter Van Zant. You can find this review on our website. Next month Frank Chance will be reviewing one of his favorite books, the Effective Executive, by Peter Drucker.

- The Semiconductor Business News website (www.semibiznews.com/) is a great place to check industry-related headlines. Topics are grouped by day, and within each day are grouped by the categories Manufacturing News, Business News, and Product News. This makes it easy to tell what's new since you last checked the site.

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