FabTime Cycle Time Management Newsletter

Volume 1, No. 3 June 2000

Information

Mission: To discuss issues relating to proactive wafer fab cycle time management.

Publisher: FabTime Inc. FabTime sells cycle time management software for wafer fab managers.

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Welcome

Welcome to the third issue of FabTime's Cycle Time Management Newsletter! We are now up to 119 subscribers, and I again thank those of you who forwarded the previous issues to other people within your companies. I find it a nice validation that people consider the newsletter worthwhile. I hope it will continue to grow.

In this third issue, the theme is Little's Law, the mathematical relationship between cycle time and WIP. Although most people are familiar with the idea of Little's Law, we thought that it would be a good idea to re-acquaint you with the full definition. It's an important principle underlying factory behavior, and we'll refer back to it when discussing other topics in the future.

As always, we welcome suggestions for future newsletter themes, and contributions in the way of news, questions, book recommendations, etc.

Thanks for participating! - Jennifer

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Definition of the Month

Little's Law - The relationship between cycle time, WIP, and throughput

The relationship between cycle time and WIP was first documented in 1961 by J. D. C. Little. Little's Law states that at a given throughput level, the ratio of WIP to cycle time equals throughput, as shown in the formulas below:

Throughput = WIP / Cycle Time

Cycle Time = WIP / Throughput

In other words, for a factory with constant throughput, WIP and cycle time are proportional. Frank Chance suggested the following intuitive example for understanding Little's Law.

- Suppose you have a train-track from San Francisco to New York City.
- Suppose it takes 3 weeks for a train to go from SF to NY.
- Suppose the route is initially empty.
- Suppose each Sunday night a train leaves SF for NY.

- Then in week 1 you have 1 train on the route (WIP = 1)
- In week 2 you have 2 trains on the route (WIP = 2)
- In week 3 you have 3 trains on the route (WIP = 3)

At the end of week 3 (and every week thereafter) a train arrives in NY, but a new train is added in SF, so you always have 3 trains on the route (WIP 3). And we can see that:

(WIP) = (rate that work enters the system) * (system cycle time) = (1 train per week) * (3 weeks) = 3 trains.

Now suppose that demand is so great that the company decides to run daily trains, e.g. the rate that work enters the system rises to 7 trains per week. But suppose as a consequence of more trains on the route, the maximum speed is lowered on the route (for safety) so that it now takes 5 weeks to complete the trip.

Looking again by week:

- Week 1: 7 trains on the route
- Week 2: 14 trains on the route
- Week 3: 21 trains on the route
- Week 4: 28 trains on the route
- Week 5 (and every week thereafter): 35 trains on the route

So again we see that

(WIP = 35 trains) = (rate that work enters = 7 trains / week) * (system cycle time = 5 weeks)

If we apply this rule of thumb to wafer fabs, suppose we have a fab that is starting 5,000 wafers per week, and is running a 4-week cycle time on average. So we can immediately guess that:

WIP = (5000 wafers per week) * (4 weeks) = 20,000 wafers.

But this assumes that each wafer goes entirely through the fab. Unless yield is 100%, this is not true. How can we correct for this? Think again of the trains, except now each train is a Lot, and each car is a Wafer. Suppose each train (Lot) is composed of 10 cars (wafers). And suppose that in Kansas City, the train loses enough passengers so that it can drop half of it cars. If we want to apply Little's Law on a train-car basis, we have:

WIP (cars) = (rate that cars enter the system) * (average system cycle time FOR CARS).

Well the system cycle time FOR CARS is not 5 weeks. Since half of the cars are dropped in Kansas City, we need to include that in our average. Suppose that it takes 3 weeks to go from SF to KC, then the remaining 2 weeks to go from KC to NY. So

Average system cycle time FOR CARS = 1/2 * (3 weeks) + 1/2 * (5 weeks) = 4 weeks.

So we have

WIP (cars) = (7 trains per week * 10 cars per train) * (4 weeks) = 70 cars per week * 4 weeks = 280 cars

Similarly in a wafer fab, if you want to apply Little's Law on a wafer-basis and need to correct for WIP, the trickiest part is calculating the average system cycle time for ALL WAFERS, including those that are scrapped.

For our example before (5,000 wafer starts per week, 4 week cycle time), if the overall average system cycle time for all wafers turns out to be 3.5 weeks, then we get

WIP (wafers) = (5,000 wafers per week) * (3.5 weeks) = 17,500 wafers

So in fact the number of wafers in the fab at any given time should really be closer to 17,500 than to 20,000. Again, this is primarily a rule of thumb, since it applies on an average basis, and day-to-day variability could cause it not to hold exactly at any given instant. But it usually gets you into the ballpark of the right answer.

Another nice rule of thumb that immediately comes from Little's Law:

If you can cut cycle time by 10%, you should see a corresponding 10% reduction in WIP:

OldWIP = (start rate) * (old cycle time)
NewWIP = (start rate) * (new cycle time)
= (start rate) * (old cycle time * 90%)
= 90% * (start rate) * (old cycle time)
= 90% * OldWIP.

Keep in mind that Little's Law doesn't say that WIP and cycle time are independent of start rate. Little's Law just says if you have 2 of these three numbers, you should be able to solve for the remaining one. The tricky part is that cycle time and WIP are really functions of the start rate. So changing the start rate in fact changes all three parameters, but Little's Law should hold for the new numbers.

For another explanation of Little's Law, and some graphs, see FabTime's cycle time tutorial, at www.FabTime.com/ctwip.htm.

Discussion Question Responses

Last month's question was "What can be done to reduce variability in process times?" Philip Ong, from Intarsia Corporation, took the time to send me his responses to the questions from both the first and second issues. His comments are included below:

Cycle Time and Variability

"Cycle time is a function of many things as you have mentioned. Therefore, what contributes most to variability?

I believe it's the lack of understanding of the process as a whole, from how a lot is started to the time it is shipped to the customer. As a result, a lack of understanding contributes to high variability in cycle times. This includes all of the factors you have mentioned and more. Any one of those factors can be the one with the most variability.

The overall measurement is in process capability. For example, what are the performance metrics to on-time-delivery, accuracy of forecasts and planning, fab process yields and reworks, equipment uptime, etc.?

It is the way you plan, execute, review the results, and plan for continuous improvement. I have seen significant cycle time reductions as a result of improvements in all of the above areas. For example, if you are measuring cycle time from the moment you start a lot of material, why start the lot if the process or piece of equipment that is required is down? Some people will make these starts to show that the overall activity of the fab was made (getting credit based on move-ins to an operation), but in reality an input was made and no real activity was made. The net is an increase in cycle time because of poor planning and process or equipment downtime issues. As a result, the material will sit at an operation that is down. Other examples are poor process capability where process test runs must be made before committing the material to ensure good product when processed.

With that all said, I would state the highest variability goes to WIP priorities / lot starts based on customer demand / sales forecast, WIP inventory, fab process capabilities, equipment uptime, then equipment utilization. I don't believe the question can be answered with a yes/no or with one single factor."

Process Time Variability

"To answer your second question (reducing variability in process times), my simple answer is understand the process and use SPC (statistical process control) and design of experiments (DOEs) to optimize the overall process.

This concept is applicable to fab as well as planning and other areas that can affect the overall cycle time. This means understanding what are the elements of cycle time and how they can be reduced. For example, understanding your lot starts, process & equipment bottlenecks in the fab, process capability / stability, etc. can help you identify areas for improvement / reduction in variability. Using the concepts of SPC and DOEs can help identify variability and help in its reduction."

FabTime Response

Philip's response to the first question, about what contributes most to variability in a wafer fab, points to the importance of consistent performance measures. People will tend to work towards whatever they are measured against, and inconsistent, or poorly chosen, performance measurement systems can lead to detrimental behavior. There's actually a story (probably highly exaggerated) about a fab that measured performance based on starts - at some point a whole slew of blank wafers were found up above the ceiling tiles of the fab. They were started!

We also agree with Philip's point that in order to improve process time variability, you first need to do some analysis to understand the behavior in your fab. Once you do understand where the problems are, here are a few suggestions for reducing process time variability:

- Smooth throughput at specific problem operations.

- Eliminate large minimum batch size requirements for all but very highly loaded tools.
- Cross-train equipment maintenance personnel, to reduce long delays waiting for the right repair person.
- Reduce tool dedication for problem tools.
- Cross-train regular operators to handle more types of equipment, and to balance schedules.
- Change preventive maintenance schedules to minimize variability.
- Modify setup avoidance policies to ensure that low-volume products are not excessively delayed
- Reduce transfer lot batch sizes.
- Modify lot release policies to smooth flow through the early steps of the process (lower variability).
- Explore process changes to eliminate operations that can only be done on a single piece of equipment.
- Explore batching rules, to make sure that all lots that can be batched together are batched together.
- Check batching and setup assumptions for rework wafers.

The above suggestions are discussed in more detail in our paper from last month's MASM 2000 conference (www.fabtime.com/abs_MASM00.htm). These suggestions were collected from various recent papers on the subject, several of which can be requested from our website by going to www.FabTime.com/request.htm. Infineon Technologies has done some especially good work in this area, and Steven Brown and his team have been generous enough to make many of their papers available to us.

New Discussion Question

What topics would you like to see covered in this newsletter? Send us your questions or suggestions, and we'll be happy to try to include them. This isn't really a discussion question - but we've had rather low response rates to the discussion questions, so I'm instead just asking if anyone has things they would like to see us write about. Thanks!

Community News/Announcements

SEMICON West

SEMICON West will take place in San Francisco and San Jose next month. The Wafer Processing sessions will take place at the San Francisco Moscone Center July 10-12, while the Test, Assembly and Packaging conference will be in San Jose from the 12th-14th. The conference is, of course, "the world's largest international tradeshow and conference dedicated to semiconductor equipment, materials, suppliers and services." FabTime's founders, Frank Chance and Jennifer Robinson, will be at the Wafer Processing conference, and we would welcome the opportunity to meet any of you who are also planning to be there. If you're interested, please look for us. We don't have a booth this year, but we've reserved a room at the nearby Palace Hotel where we can offer hospitality and software demos. You can leave us a message at the Palace (415-512-1111, under Jennifer Robinson), or try our cell phones (602-284-4726: Frank, 617-510-5179: Jennifer). We hope to see some of you there!

MASM Lab

The following announcement was contributed by John Fowler of Arizona State University:

"The Modeling and Analysis of Semiconductor Manufacturing (MASM) Laboratory at Arizona State University was created with the purpose of determining how to use operations research and statistical tools and techniques to improve the cost effectiveness of semiconductor manufacturing. The lab is housed in the Industrial Engineering department at ASU. Professors John Fowler and George Runger are co-directors of this lab. Each has extensive industrial experience; Prof. Fowler spent 4.5 years at SEMATECH, 1.5 years at AMD, and 8 months at Intel as a visiting scholar; Prof. Runger spent 6 years at IBM. The lab has done research for Amkor, Infineon Technologies, Intel, Motorola, National Science Foundation, PRI Automation, SEMATECH, Semiconductor Research Corporation, ST Microelectronics, and Tefen.

Problem areas that are currently being studied in the MASM lab include: 1) factory (both fab and assembly/test) performance analysis; 2) factory planning and scheduling; 3) equipment productivity methodologies; 4) statistical process control; 5) design of experiments; 6) data mining; and, 7) supply chain management.

The lab also acts as a clearinghouse of information on issues related to modeling and analysis of semiconductor manufacturing. This is done primarily in three ways: 1) through a web-based bibliography (see www.eas.asu.edu/~masmlab) that can be searched by application area (e.g. scheduling), by performance measure (e.g. cycle time), by technique (e.g. simulation), by author, by year, etc.; 2) through a collection of data sets of real factories that can be downloaded from www.eas.asu.edu/~masmlab. The data sets contain enough information that reasonably accurate simulation models can be built; and 3) by hosting an annual international conference on modeling and analysis of semiconductor manufacturing (see www.eas.asu.edu/~masmlab/masm2000)."

We at FabTime think that the MASM lab has lots of great resources - and recommend that you take a look at their website.

FabTime welcomes the opportunity to publish similar announcements for other companies. Simply send them to Jennifer.Robinson@FabTime.com.

FabTime Recommendations

■ FabTime's book of the month for June is the Effective Executive, by Peter F. Drucker. You can find this review on our website.

■ The INFORMS College of Simulation website now has electronic copies of all the papers from the Winter Simulation Conference proceedings from 1997-1999 at www.informs-cs.org/wscpapers.html. The papers can all be downloaded in PDF format. For 1999, the abstracts are also available in HTML, making it easier to decide which papers might be interesting enough to download. There are lots of great papers about cycle time as well as semiconductor manufacturing.

■ The Intel Technology Journal (www.intel.com.my/technology/itj/index.htm) is another interesting online resource. All of the articles are well-formatted in html, and the site is easy to navigate. The articles tend to be more about the technology and process side of things than the manufacturing side, but the Q4 1998 issue is entirely dedicated to manufacturing.

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