FabTime Cycle Time Management Newsletter

Volume 3, No. 6 June/July 2002

Information

Mission: To discuss issues relating to proactive wafer fab cycle time management.

Publisher: FabTime Inc. FabTime sells cycle time management software for wafer fab managers.

Editor: Jennifer Robinson

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Contributors: Maneck Bhujwala; John Fowler (ASU); Guido Dietz (Infineon Technologies); Hung-Nan Chen (Motorola); Andy Egan (Productivity Partners, Inc.); Douwe van Engen (Philips Semiconductors); Daren Dance (WWK); Eric Olsen (Ohio State University)

Welcome

Welcome to Volume 3, Number 6 of the FabTime Cycle Time Management Newsletter. In this issue, we have subscriber discussion related to wafer starts methodologies, operator modeling, operator dedication, ramp planning, cost of scrap, and recipe management. Most of the comments were submitted in response to previous reader questions - my thanks to all who took time out of your busy lives to contribute to our discussion!

In this month's main article, we propose three distinct cycle time management styles, and describe how each can be used to improve cycle time. We have named these three styles: The Traffic Cop; The Shepherd; and The Relay Coach. These are management styles we have observed in real fabs, although the names and descriptions are our own. Each style is suited to a particular cycle time focus. Traffic Cops control starts and WIP flow for production lots. Shepherds prevent engineering lots from disappearing onto shelves and hiding in corners. Relay Coaches ensure that critical hot lots are handed smoothly from one operation to the next. We hope that you will find the article useful. Graphical examples, using charts from FabTime's software, can be found on our website, at www.FabTime.com/ctmstyles.htm.

Fablime

325M Sharon Park Dr. #219 Menio Park CA 94025 Tel: 408 549 9932 Fax: 408 549 9941 www.FabTime.com Frank and I hope to see some of you at SEMICON West next month (announcement below). The next newsletter is scheduled for publication in early August.

Thanks for reading! -- Jennifer

Community News/Announcements

FabTime at SEMICON West

FabTime's Frank Chance and Jennifer Robinson will both be attending SEMICON West in San Francisco July 22nd and 23rd. If any newsletter readers are planning to attend SEMICON West, and would like to meet with us, please let us know. Just send email to Jennifer.Robinson@FabTime.com or Frank.Chance@FabTime.com, and we'll be happy to arrange a meeting. Hope to see you there!

Semiconductor FabTech Article Published

Our paper "Understanding and Improving Wafer Fab Cycle Times" recently appeared in Volume 17 of Semiconductor FabTech (www.FabTech.org). You can find an abstract to the paper at www.fabtime.com/ abs_FabTech02.htm.

Engineer Available for Employment

Maneck Bhujwala sent us the following announcement: "Software Quality Assurance and Development Manager/Engineer with experience in semiconductor Fab Automation (Computer Integrated Manufacturing) and Design Automation applications, available for immediate employment. Call Maneck Bhujwala at (408) 270-9173 or send email to maneck_bhujwala@mindspring.com."

FabTime welcomes the opportunity to publish community news and announcements. Simply send them to Jennifer.-Robinson@FabTime.com.

Subscriber Discussion Forum

Wafer Starts Methodologies

In response to last month's question about wafer starts methodologies, John Fowler of Arizona State wrote: "Another fine issue...... The following paper will soon appear in the journal Production Planning and Control. I would be happy to send a copy to any interested parties: Fowler, J.W., Hogg, G.L., and Mason, S.J., "Workload Control in the Semiconductor Industry", Production Planning and Control, to appear." This paper is about both order release methodologies and dispatching strategies. You can request this paper from John at John.Fowler@asu.edu.

Operator Modeling

Guido Dietz of Infineon Technologies wrote in response to the question about

modeling operators: "I have got an interesting addition to your answer concerning Operator Modeling. There was a presentation on this year's ASMC in Boston (attached)."

H-N Chen and R. Dabbas, "Modeling Staffing Requirements within a Semiconductor Manufacturing Environment," Proceedings of the 2002 Advanced Semiconductor Manufacturing Conference, Boston, MA, 234-239, 2002.

If any subscribers would like a PDF copy of this presentation, send email to Jennifer.Robinson@FabTime.com. The full paper is available in the ASMC proceedings. The first author, Hung-Nan Chen of Motorola, added these comments:

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"This paper takes similar approaches (capacity, queuing, and simulation) seen in Factory Explorer, Raviv 1995/TEFEN, AGI, and references in the paper but details on implementation of these methods. The technology is not new but the readers will benefit from seeing how these methods were implemented in a fab."

Operator Dedication

Responding to both Rick Alexander's previous comments on tool dedication, and last month's question about planning for the number of operators, Douwe van Engen, Waferfab RF modules, Philips Semiconductors Nijmegen, The Netherlands wrote:

"Now we are struggling with the fact that there is a trend going on in our factory to make the operators more and more multiple employable (autonomous groups). This is not limited to make them multiple skilled for operations, but also for activities as simple preventive maintenance, making of progress reports and dispatch list, and training of other operators. It feels that those extra duties will have more management attention than moving of lots.

The question we are asking ourselves is: "how far can you go with making the operators multiple employable, without losing the benefits of multiple skilled operators in terms cycle time (lower variability). Is there an analogy with the example of Rick Alexander in Fabtime Cycle Time management Newsletter Volume 3, Number 4?"

Do you know what trend is going on in other semiconductor factories with respect to this topic?

Hopefully you can help us solving this dilemma."

FabTime Response:

You raise an interesting issue. I'm afraid I haven't heard anything about this type of operator training (going beyond traditional operator duties), and so I don't have any answer to "how far can you go?" I think that it depends on the size of your factory, and on how much slack capacity the operators have. If your operators end up very highly loaded due to the additional activities, then you'll end up with cycle time delays due to tools being ready for processing when no operator was available. The idea behind ordinary cross-training of operators to be able to use multiple tools is much like the idea of reducing tool dedication, and should improve cycle times in the same way. However, if you include training for other types of activities, to the point where the operators are sometimes not available when the tools need them to be, then I think you can hurt cycle time. For cycle time, you want to maximize the amount of time that operators are available to process lots at tools, and to transport lots, so that lots are never delayed because of operator unavailability. I do think that this is analogous to what Rick Alexander had to say about tool dedication. In your case, delays while the operator finishes other tasks are analogous to the setup times on equipment. But really, we can't speak to the trend in the industry on this. Perhaps our other subscribers will have something to add.

Ramp Planning

Andy Egan of Productivity Partners, Inc. wrote: "One of your correspondents in your newsletter asked about Ramp plans. We examined this question at Siemens NTS and have since looked at it again. In both cases we purpose built the models, verified them at constant output, then started the ramp plan. In both cases implementing the plan as originally envisioned in the model would probably cause shortterm but serious cycle time problems. We

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NTS and have since looked at it again. In both cases we purpose built the models, verified them at constant output, then started the ramp plan. In both cases implementing the plan as originally envisioned in the model would probably cause shortterm but serious cycle time problems. We were asked to run alternative plans and to suggest ways of getting the required production. After some experiments we found a combination that would probably achieve the production required without the cycle time penalty. In our experience each of these models needs to be built individually. The first model took 3 weeks but with input data already known, the second took six weeks including data collection. These models were built on AutoSched and Factory Explorer respectively and in both cases proved to be representative of the real system."

Treating Scrap in Product Costing

Daren Dance of WWK sent the following comments on last month's question about treating scrap in product costing: "I have found the yield losses generally stem from two sources: either the process is out of control or the process capability allows some product/process mismatch. For leading edge devices the risk of product/ process mismatch may be quite high. In prior product costing, I have included this mismatch risk as a part of the cost of the product. We estimate the product/process mismatch risk using several published yield models and also looking at previous yield history. This helps to justify the higher price for new products that exceed the mainstream performance capabilities of the existing process."

Recipe Management

Another subscriber wrote: "Here at my company we have a problem with recipe management. There are certain tool groups that have literary thousands of recipes. There are product specific recipes, tool

specific recipes, and lot specific R&D recipes, among others. There is a lot of recipe duplication. And there are several people who have rights to make changes, making it difficult to know who did what, when. A good example of the problems that poor recipe management causes occurred today. We have three tools that can run recipe X, but for some reason, for two days, operators were only using one of the tools, and WIP was piling up. Upon investigating we found out that someone had disabled the recipes from the other two tools, but didn't inform others of the change. This happens all the time, in different areas of the fab. And it negatively affects cycle time. Is this something that we all live with or has someone developed a good system for recipe management?"

CT Benchmarking for GaAs Fabs

Eric Olsen, a researcher at Ohio State University, submitted the following question. "We are seeking viable benchmarks and benchmark criteria for cycle time in GaAs fab processes. It is our feeling that "working days/layer" is a problematic criteria in processes that use smaller wafers, suffer more breakage, and have an order of magnitude fewer layers than silicon processes.

A. Does anyone have a standard for calculating theoretical or intrinsic cycle time for these types of processes?

B. We feel that viable benchmark criteria should include wafer size, lot size, breakage handling policy (to process or not, min size, etc), and number of active and passive layers on the final die. Is this a complete enough set of criteria for making CT comparisons between processes? If not what else should be considered?

C. What constitutes typical or "best-inclass" cycle time performance for GaAs fab processes?"

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Cycle Time Management Styles

Introduction

In this newsletter, we've talked about many factors in a wafer fab that affect cycle time - utilization, lot size, hot lots, tool dedication, variability, and so on. Understanding these issues is certainly key to improving cycle time. Two months ago, Dan Siems wrote about why managing and improving cycle times is difficult (the core conflict), and proposed some key elements to a cycle time improvement program. As it was meant to, this article left us thinking: "OK, but what do you do next? On a day to day basis, how do you manage and improve cycle times?" Last month, we highlighted some of the financial benefits that stem from cycle time improvement. In this issue, FabTime proposes three distinct cycle time management styles, and describes how each can be used to improve cycle time under certain conditions. We have named these three styles: The Traffic Cop; The Shepherd; and The Relay Coach.

The Traffic Cop

The Traffic Cop's goal is to monitor and manage starts, to control equipment utilization. What the Traffic Cop does is:

1. Identify the fab bottleneck with a capacity model (usually spreadsheet, queueing, or simulation-based).

2. Control fab starts to keep the bottleneck utilization below 85%.

3. Monitor WIP turns (as shown in the chart below) in the fab to avoid unexpected utilization spikes.

This methodology requires that the Traffic Cop has access to an accurate capacity model, and has management authority for both starts plans and performance measurements.



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Mathematical Justification and Impact

As we have discussed in earlier issues, utilization is generally the most significant driver of cycle time. This is based on wellknown mathematical formulas. Cycle time at most toolgroups is proportional to rho/ (1 - rho), where rho is the toolgroup loading. The higher the loading of the toolgroup, the higher the cycle time. For the fab as a whole, cycle time is highly dependent on the utilization of the bottleneck. As rho approaches one, 1/(1 - rho)approaches $1/(0) \sim =$ infinity. So, the idea behind this traffic management style is to control rho, so that 1/(1 - rho) does not become unacceptably large.

Example

For a graphical example of the Traffic Cop method, applied using FabTime's cycle time management software, please go to www.FabTime.com/traffic_cop.htm.

The Shepherd

The Shepherd's goal is to monitor and manage inactive lots to control variability in the fab. Inactive lots are lots that have been at their current operation, without moving, for some period of time that the fab defines as "inactive." The general methodology for what the Shepherd does is:

1. Set a goal for maximum inactive time per lot (e.g. 10 hours).

2. Monitor the number of inactive lots (both the total in the factory, as shown in the chart below, and the numbers by area and/or key toolgroups).

3. Identify and address the root causes for lot inactivity, to prevent situations from recurring.



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This methodology requires that the Shepherd has access to accurate, real-time reporting of inactive lots, and has management authority for scheduling and dispatching decisions as well as performance measurements.

Mathematical Justification and Impact

Cycle time is a function of utilization, arrival process variability, process time variability, and number of tools in each tool group. Focusing on inactives reduces variability in the fab. Processing the inactive lots first at an operation translates to processing the oldest lots first, and drives towards first-in-first-out dispatching. In mathematical terms, focusing on inactives at an operation reduces the coefficient of variation of arrivals to downstream operations, and thus reduces cycle times. As a side benefit: there have also been strong arguments made that the longer a lot sits in the fab without being worked on, the more likely it is to have yield problems. Therefore, reducing the number of inactives may improve yield.

Example

For a graphical example of the Shepherd method, applied using FabTime's cycle time management software, please go to www.FabTime.com/shepherd.htm.

The Relay Coach

The Relay Coach's goal is to monitor and manage queue time to control hot lot cycle times. What the Relay Coach does is:

1. Set a goal for the maximum hot lot queue time (e.g. ¹/₂ hour). This might vary for different types of hot lots.

2. Establish buy-in from key resources in the production organization.

3. Use an automated tracking and paging system to notify the Relay Coach if the queue time goal is exceeded for any hot lot.

This requires that the Relay Coach has access to an automated tracking and alerting system, significant management support, and a tactical communications plan (policies, escalation, directory, etc.).

Mathematical Justification and Impact

As we discussed in Issue 3.02, the presence of hot lots, with low cycle times, will tend to increase the cycle times of regular lots. However, if the number of hot lots is minimal (no more than 5%-10%), then the inflation of non-hot-lot queue time will be relatively small. The relay coach approach requires very close monitoring of the hot lots, above and beyond the simple use of lot priorities. This approach is thus only appropriate for a very small number of lots - perhaps 5 to 15 lots at one time. By only managing a few lots at one time with this method, it is possible to have very low cycle times for a few critical lots, without much adverse impact on the other lots.

Example

The chart on the next page shows the lot history for a critical lot, broken out into queue time vs. process time. For a more extended graphical example of the Relay Coach method, applied using FabTime's cycle time management software, please go to www.FabTime.com/relay_coach.htm.

Conclusions

This article proposes three styles for managing and improving wafer fab cycle times. The Traffic Cop approach involves managing starts to control utilization and thus keep cycle times lower for all lots. The Shepherd approach involves managing inactive lots, to reduce variability in the fab, and thus reduce both cycle times and cycle time variability. The Relay Coach approach involves focusing close attention on a small number of hot lots. This gets those particular lots through with very low cycle times, though at the expense of other lots. These approaches all require access to

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accurate, real-time data about fab behavior, along with management authority to make recommendations or changes. These approaches can be used together (with some trade-offs required), and can be used in conjunction with other cycle time improvement efforts such as variability reduction programs. The idea of the article is to give examples of specific approaches that we have seen generate good results in real fabs.

Closing Questions for FabTime Subscribers

How do you manage cycle times in your fab, on a day-to-day or week-to-week basis? Do you recognize yourself in any of the three management styles defined above?

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References

■ This article is derived from a talk that Frank Chance gave at Arizona State University in January of this year. For a copy of the slides, send email to Frank.Chance@FabTime.com.

■ For an example of the Relay Coach type of approach (as applied by AMD), please see the paper M. Hillis and J. K. Robinson, "Super-Expediting in a 0.18 Micron Wafer Fab," Proceedings of the 2002 Modeling and Analysis for Semiconductor Manufacturing Conference (MASM 2002). Tempe, AZ, April 10-12, 2002. You can request this paper from FabTime at www.FabTime.com/request.htm.

FabTime Recommendations

Back of the Envelope Approximations

The idea behind this site is that sometimes you don't need exact calculations. Sometimes you need a rough estimate, to get an idea of the scale or scope of something. This is why "back of the envelope" calculations are used in the first place. The Back of the Envelope website contains a collection of these types of rough calculations and approximations. For example, there's a picture that shows you what a dot for every second in the day looks like, and one that shows what a million dots look like. There are also sections on rounding, exponential notation, power of ten calculations, etc. This site is at www.vendian.org/ envelope/. We learned about this site from the Librarians' Index to the Internet (www.lii.org).

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