FabTime Cycle Time Management Newsletter

Volume 2, No 6, July 2001

Information

Mission: To discuss issues relating to proactive wafer fab cycle time management.

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Welcome

Welcome to Volume 2, Issue 6 of the FabTime Cycle Time Management Newsletter. We've had a big jump in subscribers since the last issue, from 377 to 452. Many thanks to all of you who have subscribed, and who have passed the newsletter on to others within your companies. This month we have a large number of responses, announcements, and recommendations submitted by various subscribers. Thanks to all who've helped to make our newsletter more interesting by taking the time to contribute something.

This month FabTime is happy to report that as of July 12th our software system had been running continuously in real time for more than 100 days at Headway Technologies in Milpitas, CA. More information is available in the Community News/Announcements section.

This month's main article is titled: "What is One Day of Cycle Time Reduction Worth?". The article was written by Frank Chance, with assistance from Stuart Carr (consultant and FabTime affiliate), and Ken Beller. Frank started thinking about this question because, as President of a cycle time management software company, he is frequently asked about the dollar benefit of cycle time reduction. This article outlines several potential ways to quantify this benefit, and focuses in particular on the timely issue of inventory write-off during an industry downturn. The article references an Excel-based cycle time payback calculator which you can download from FabTime's website. (Editor's Note: This example spreadsheet was removed from FabTime's website on 5/15/02, and superceded by the spreadsheet described in newsletter issue 3.5.) We think that you'll find this article both relevant and interesting.

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Responses to Previous Newsletter Topics

Ideal Cycle Time Reference (OEE)

John Fowler (ASU) wrote: "Another great issue. If the number of subscribers continues to increase at the current rate, my model says that there will be more subscribers than people living in the state of California by the year 2025.....

In regards to the "ideal" process time, there is now a SEMI standard that addresses this issue, E79. It defines: Intrinsic Equipment Efficiency [IEE] - (time divided by time) - a measure of equipment productivity that considers the combined effect of rate efficiency losses, recipe design, and equipment design. IEE is based on value-added in-process theoretical production time for actual units and production time. It can be calculated by dividing the actual processing time by the total productive time."

OEE Calculation Clarification

Another newsletter subscriber wrote: "I've read issue 2.4, which was very interesting and was "just in time" for me. I was looking for material on OEE calculations and the references you gave were great help. I have though a question I was unable to answer, and I was hoping you could refer me to further information. It has to do with the third component of OEE which is Quality rate. Are we looking for the wafers scraped after the specific tool we are looking at, and regarding reworks, should I look for the # of reworks processed by the tool in question?"

FabTime consulted with V.A. Ames (one of the authors of the SEMATECH OEE Guidebook) on this question, and V.A. responded with the following:

"All OEE calculations should be in regard to the tool that is affected by the loss, so yes any rework that is run by the tool being measured should be considered a rate of quality loss, even though the cause may have been from another tool. Anything we run through the tool more than once is a loss of efficiency.

Quality can be thought of in the same way, but it usually mans that we have to shift paradigms. I say "usually" because we would like to consider the quality loss on the tool that caused it, but that is very hard to capture in most instances. We find out about the quality further down the manufacturing process in a measurement step, probe test, or even final test.

Therefore, I recommend measuring the quality loss at the operation that is impacted (measurement tool, probe, final test, etc). This is much easier to capture and shows the true efficiency loss on the tool that is impacted the most. All fabs have stringent quality initiatives to identify root cause and strive to fix the tool that caused the problem, so having it referred back to that tool for OEE is not all that useful. Besides the number is usually so small, the loss of efficiency is negligible.

I have also been planning to write you a note (when I find the time) on the importance of using SEMI E79-0200 as the reference for OEE instead of the SEMATECH OEE guidebook. One of the major differences is in the quality measurement. The guidebook treats all quality loss equal, but SEMI E79-0200 takes into consideration the greater efficiency loss of scrapping a 25 wafer lot that takes 45 minutes per wafer versus a scrapped 25 wafer lot that only takes 5 minutes per wafer.

The guidebook was our first attempt at trying to standardize an OEE equation for the SEMATECH member companies,

based on our learning at that time. SEMI E79-0200 is an "industry" standard that addresses many of the unknowns in 1995, including the calculations for multi-chamber tools with parallel processes, addressing the issue of "idle time" due to no WIP, and other questions that have been brought up in your newsletter."

What is One Day of Cycle Time Reduction Worth?

Introduction

This has been a difficult question to answer for wafer fabs. Most people implicitly understand that a one-day reduction in cycle time is good. But turning that implicit understanding into an explicit dollar benefit is hard work. Reduction in cycle time is generally believed to have the following virtuous effects:

- Shorter R&D lot cycle time --> Increase R&D learning cycles --> Shorter time to new-product introductions --> More design wins --> First to ramp manufacturing volume for new products --> Larger market share --> Higher profits.

- Shorter volume lot cycle time --> Increase volume manufacturing learning cycles and reduce manufacturing WIP --> Fewer ECN Losses --> Lower total costs.

- Shorter volume lot cycle time --> Reduce manufacturing WIP --> Reduce inventory holding costs --> Lower total costs.

- Shorter volume lot cycle time --> Increase output without buying capital equipment --> Reduce capital costs and minimize equipment installation delays (improve volume ramp) --> Lower total costs and higher profits.

What we're going to discuss today is a slightly different benefit, which is especially relevant for today's business climate:

- Shorter volume lot cycle time --> Smaller safety stock requirements for post-fab supply chain --> Smaller risk of inventory writeoff during industry downturn --> Lower total costs.

To quantify this benefit, we need to think about the impact of fab cycle time on the downstream supply chain (i.e. the wafer fab's customers, be they internal or external). Pick up any edition of the Wall Street Journal and you're likely to read another story about a high-tech company taking a loss of many millions of dollars to writeoff inventory that cannot be sold. For example, one well-known company this week announced a $300 million dollar inventory writeoff.

How does this happen?

Consider a perfect supply chain -- each manufacturing module and transportation link has zero cycle times. When a customer orders a product, this demand is propagated up the supply chain instantly. The desired product is then built instantly, and then delivered to the customer. In this scenario, there would never be any unsold inventory or inventory writeoffs.

In any real supply chain, however, the manufacturing modules and transportation links have non-zero cycle times. Unless the customer is willing to place an order and then wait while the supply chain works all the way from the beginning to produce the desired product, there must be some accumulation of inventory within the chain to cover this demand.

How do supply chain planners decide how much inventory to hold? In general, this is a thesis topic in and of itself. But it's not hard to draw some general conclusions. Consider a post-fab die bank that is used to supply demand for individual devices. If the fab's cycle time is extremely short and extremely predictable, then we don't need to hold much inventory in the die bank -- when the die bank starts running low on a particular device, we can start more wafers into the fab, and before too long, replenish our die bank. We can decide when to start wafers, and how many wafers to start, based on the fab cycle time and our expected demand. But if the fab's cycle time is extremely long and extremely variable, then we need to hold extra safety stock in our die bank, to supply customer demand during the fab's long (and unpredictable) cycle time.

So we can safely conclude:

--> Longer fab cycle times cause planners to hold more safety stock in the post-fab supply chain. --> When a downturn occurs, more safety stock implies higher inventory writeoffs.

And thus:

--> Longer fab cycle times lead to higher inventory writeoffs.

Quantifying the Impact

To quantify the impact of cycle time reduction on inventory writeoffs, we'll use a popular method for inventory planning known as the "(R,S) Periodic Review Policy" (see section 17-8 of Wayne Winston's "Operations Research" (2nd ed) for the details of this policy). To ease our discussion, we have created a spreadsheet that automates the calculations and placed this spreadsheet on the FabTime website at www.FabTime.com/ctbenefit.htm. You can use that spreadsheet to follow along here.

Let's assume a wafer fab with the following parameters:

- Baseline Cycle Time: 60 days
- Improved Cycle Time: 59 days
- Weekly Wafer Outs: 2000
- Good devices per Wafer: 25
- Days between post-fab order review cycles: 30 (e.g. the die bank is reviewed monthly and wafer starts are planned from this review)
- Fab production cost: $40/device (equivalently, price that fab would charge if die bank were operated by a separate company)
- Lost profit if die-bank is unable to supply a customer request for a particular device: $20/device
- Volatility in yearly demand for individual devices: +/- 75%
- Percent of die-bank inventory that is written off in case of industry downturn: 50%
- Holding cost percentage for die-bank inventory: 24%

Given these inputs, we would like to know how much die-bank inventory the planners will recommend (first, given the baseline cycle time, and then given the improved cycle time). From these numbers, we can calculate how much inventory would be written off in an industry downturn (again, for the baseline cycle time, and for the improved cycle time). The difference in inventory writeoffs between the baseline cycle time and the improved cycle time will be a dollar benefit of a one-day reduction in cycle time.

If you open our spreadsheet, these numbers are entered as "Scenario 1" on the "Calculator" worksheet. Now switch to the Details worksheet. The calculations under "Scenario 1" are in two columns. The first column performs the calculations for the baseline cycle time, the second column performs the calculations for the improved

cycle time. Locate the OrderUpTo row for the baseline results. The value should be 1,213,985 devices. This is the number of devices that the (R,S) policy would recommend holding in the die bank. Now consider the improved results -- the OrderUpTo value is 1,203,670 devices. The difference, 10,315 devices, is the reduction in die bank inventory attributable to our one-day reduction in fab cycle time.

Again, this benefit is not just a reflection of Little's Law (which says that cycle time and WIP are linearly related). This benefit occurs because supply chain planners can choose to hold less post-fab inventory, once they know that fab cycle times have been reduced from 60 days to 59 days.

So, it's important to remember:

--> It's not enough to reduce your fab cycle time -- you also have to let your planning organization know, or the benefit will never be realized!

Getting back to our example, we assumed that in a downturn, 50% of the die-bank inventory would have to be written off. The Details worksheet calculates this quantity and values it at cost, for the baseline case and for the improved cycle time case. The difference between these two writeoffs:

$206,298 = $24,279,692 - $24,073,394

is the benefit reported on the Calculator worksheet.

To summarize: In our example, cutting fab cycle time from 60 days to 59 days, AND getting the die-bank planners to use the new cycle time in their calculations, results in a reduction of inventory writeoff risk of $206,298.

Note: We are assuming constant fab cycle times in this model -- if we take fab cycle time variability into account, that further inflates the amount of safety stock held in the die-bank, and thus the amount of inventory writeoff risk. So, the dollar benefit reported here is a lower bound for the actual benefit (when there is cycle time variability).

Summary

Quantifying the dollar benefit of cycle time reduction is work. What we have presented today is one way to quantify the benefit of a reduction in inventory risk for the post-fab supply chain, when fab cycle time is improved. There is real money at stake here, as even a casual glance at the Wall Street Journal will verify. Every fab will be different, so we have provided a spreadsheet that automates the calculations, and lets you quickly view three different improvement scenarios on one page. Please feel free to use this spreadsheet, and to pass it along to others -- we only ask that you attribute the source, and maintain our copyright notice!

Community News/Announcements

FabTime Hits 100-Day Continuous Uptime Mark at Headway Technologies

Menlo Park, CA. July 10, 2001. - FabTime Inc. today announced that its FabTime cycle time management system at Headway Technologies surpassed the 100-day continuous uptime mark. FabTime is a cycle time management system that provides web-based access to fab performance data for Headway's fab manager and fab supervisors. During this 100-day period, FabTime served over 1,000,000 informa-

tion requests, with an average response time of less than one second. The FabTime system is powered by a Dell PowerEdge server running Microsoft Windows NT 4.0 and Microsoft SQL Server 7.0.

"FabTime has become a critical component of my daily preparation, and my managers have grown to rely on it," said Lyle Rusanowski, fab manager, Headway Technologies. "Our fab has to operate 24x7, and so do our critical software systems. It's great to know that we can rely on FabTime."

About Headway Technologies:

Headway Technologies designs and manufactures recording heads for high performance hard disk drives. Headway is a part of the TDK group of companies (NYSE: TDK), the largest independent recording head supplier to the hard disk drive industry. Headway's wafer fabrication facility is located in Milpitas, California. The company's website is located at www.Headway.com.

About FabTime Inc:

FabTime Inc. is the first company to focus solely on the challenging problem of cycle time management for semiconductor wafer fabrication facilities. Unlike traditional reporting tools, which were designed for industrial engineers and IT specialists, FabTime's software is designed for hands-on use by fab managers. The company's website is located at www.FabTime.com.

Name Change for Hyundai Semiconductor America

Arnie Stein sent us the following press release: "Effective immediately, Hyundai Semiconductor America has a new name. It is Hynix Semiconductor Manufacturing America Inc. (HSMA). The name is derived from "high electronics." The new name is part of an overall corporate restructuring that will separate the semiconductor operations from the Hyundai conglomerate. The company expects to complete the restructuring by June 2001.

Our new corporate name is intended to create an image of a company that will specialize in the semiconductor arena for the 21st century. We would like to use this opportunity to declare the worldwide and nationally independent nature of the newly spun-off group. The purpose of this change is not only to create a new image, but also to strongly encourage internal organizations to achieve much higher goals, and thus to give you high confidence in business with our company."

Book Recommendation - James Ignizio

James Ignizio wrote: "I'd also like to recommend my recent novel: GONE AWRY - a virtual tour through high tech hell, to your readers. A website for the book is at www.geocities.com/goneawry25 and the book is listed on Amazon.com and other on-line book stores.

This was my first venture, after publishing 7 textbooks, into fiction. GONE AWRY is a satire about the impact of high technology on society --- using a modern day Dante's venture into the hell of high technology as its basis. I was just informed that it is a finalist for a book of the year award presented by WRITERS' DIGEST. If nothing else, it might give your readers a welcome break from their technical reading."

Dr. Walt Trybula Receives Industry Leadership Award

He didn't submit this to us himself, but we came across the following press release on SEMATECH's website. Since Walt has been a regular newsletter contributor, we wanted to share it with you.

"AUSTIN, Texas (13 June 2001) -- Interna-

tional SEMATECH's Walt Trybula was recently honored by the Institute of Electrical and Electronics Engineers (IEEE) Components, Packaging and Manufacturing Technology (CPMT) Society with the 2001 Electronic Manufacturing Technology Award. The award is given yearly to recognize major contributions to Electronic Manufacturing Technology in fields encompassed by the CPMT society.

Trybula, an IEEE Fellow, was specifically recognized for his leadership in semiconductor manufacturing technology, and for the development of models and simulation tools which have had and will continue to have a significant impact on the semiconductor and semiconductor manufacturing packaging industries.

"It's an honor to be recognized in this way, and especially through an organization of industry peers," said Walt Trybula, a Senior Fellow at ISMT. "It's professionally rewarding to be at the center of the action and to work side-by-side with the best researchers in the world."

International SEMATECH's Chief Operating Officer Rinn Cleavelin said, "Walt brings a life of experience to International SEMATECH in several different areas, including his understanding of lithography, but more important, an understanding of how lithography fits into the economics and business of this industry."

Trybula first joined SEMATECH in 1993 as a project manager for Simulation and Modeling with responsibility for cost and flow analyses of equipment and facilities. Since then he was a senior member of the technical staff and the acting manager of the Operational Modeling department. As senior fellow, Trybula evaluates the impact on the lithography segment of the semiconductor industry as technology acceleration occurs. Trybula is also responsible for coordinating lithography cost modeling inputs to other projects to insure consistency and concurrency of the results.

Walt Trybula was presented the award during the 51st Electronic Components and Technology Conference held May 29-June 1, 2001."

FabTime welcomes the opportunity to publish announcements for individuals or companies. Simply send them to Jennifer.Robinson@FabTime.com.

FabTime Recommendations

Book of the Month

FabTime's new book of the month for July is "Clockspeed: Winning Industry Control in the Age of Temporary Advantage", by Charles H. Fine. You can find this review on our website at www.fabtime.com/clockspeed.htm. As with all of our reviewed books, we provide one-click access to the book for ordering from Amazon's website.

Andy Grove Article

Chad DeJong (Intel) recommended this Wired Magazine article to us: www.wired.com/wired/archive/9.06/intel.html. The article is titled: "Andy Grove's Rational Exuberance", and describes Andy Grove's views on the current and future state of the high-tech industry.

Cost of Cycle Time

Walt Trybula (SEMATECH) recommended an article that he co-authored, currently available at the Semiconductor International website. The article is titled "The Cost of Imperfect Wafer Environmental Control", by Devon Kinkead and Jim Mastrobuono of Extraction Systems Inc. (Franklin, Mass), and Kim Dean and Walt Trybula of International SEMATECH (Austin, Texas). This article quantifies the cost of delayed ramp-up of a wafer fab, using graphs to illustrate the reasons for the high cost of delays (when prices are dropping, as they generally are). The paper specifically outlines why the impact of a delayed introduction for DRAM has a financial consequence of $2.5M per day of delay. You can find this article at: www.semiconductor.net/semiconductor/issues/issues/2001/200106/06six0106cost.asp. Or go to http://www.semiconductor.net, and click on the link on the main page (mid-way down) for Cost of Imperfect Wafer Environment Control, Part 2. Then click on the link to part one in the first paragraph of the story. This article is from Semiconductor International, June 2001, p. 135.

INFORMS Documents on Demand

INFORMS is the professional society for operations research and management science personnel. They publish a number of well-respected technical journals, such as Management Science, Interfaces, Operations Research, Manufacturing & Service Operations Management, etc. They have recently made articles from all ten of their journals available upon request in PDF format. They charge $10 per article, and have articles from 1998 to the present available. You do not have to be a member of INFORMS to order papers. Ordering information from the INFORMS press release on this subject is included below:

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Stuart Carr
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