FabTime Cycle Time Management Newsletter

Volume 2, No 5, May 2001

Information

Mission: To discuss issues relating to proactive wafer fab cycle time management.

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Welcome

Welcome to Volume 2, Issue 5 of the FabTime Cycle Time Management Newsletter. We've now been publishing the newsletter for one year, and have decided to make this a special anniversary issue. Instead of having a new topic for the month, we've included very brief summaries of the issues sent to date, and the number of subscribers who originally received each issue. We've gone from 33 subscribers for the first issue to 375 for this issue. If these summaries inspire you to want a copy of any of the past issues, just email me to let me know, and I'll be happy to send them.

We also have in this issue a follow-up question from Bob Kotcher regarding OEE, a suggestion about a reference source for the SEMI E-10 standard on equipment states, a job change announcement from Todd Hudson, and an announcement concerning a successful scheduling project at Samsung from Rob Leachman.

Thanks for reading! -- Jennifer

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Responses to Previous Newsletter Topic (OEE)

SEMI E-10 Standard Reference

A couple of people asked us after the last issue whether they could have a copy of the SEMI E-10 Standard for equipment performance. SEMI does not allow free distribution of the full standard - you have to pay SEMI a $50 fee to download it. However, we have found an abridged description of OEE as an appendix to the SEMATECH OEE Guidebook. This Guidebook can be downloaded from SEMATECH's website for free. Not only does it provide a good overview of OEE, it provides a first-pass look at the SEMI E-10 standard. And all for the right price. You can find the OEE Guidebook at http://www.sematech.org/public/docubase/summary/2745agen.htm.

From Bob Kotcher - Headway Technologies

"Thanks for the interesting newsletter, Jennifer. I was your target audience exactly: I had a familiarity with OEE but did not have all the nuts & bolts to calculate it precisely on my own. Now I do! I made a note to include an OEE calculation in my Wintersim paper.

However, one thing I'm still curious about is "rate efficiency," which you define as "ideal process time over actual process time." Since almost every part of every process within a tool could possibly be improved (bound only by the laws of physics), how do we determine "ideal" process time? I guess we could pretty clearly discount robot moves and pumping and venting times, for example, as well as inefficiencies caused by less than full batches, but if we, say, count only actual sputtering time in a tool as "ideal," well what about a process improvement that could be made within this tool to speed the deposition rate? Wouldn't that mean that the current actual sputtering is "inefficient" to some extent? And to what extent, given that we probably don't know what exactly is the absolute fastest processing time as dictated by the laws of physics?

I think that the answer to this question would be a popular addition to your next newsletter. Thanks!"

FabTime Response:

Bob's question highlights an area in which our previous discussion on OEE was unclear, that of the definition of "ideal" process time. The SEMATECH OEE Guidebook defines the ideal process time as that defined by the equipment supplier's specification. In theory it would be great to keep pushing to reduce process times all the time, until some theoretical limit was reached. In practice, using the supplier-specified standard for the ideal processing speed should be quite sufficient for most OEE applications. Sorry that we weren't clear about this before.

FabTime Newsletter Retrospective

Volume 1, Number 1 - The Hawthorne Effect (33 subscribers)

The Hawthorne Effect is named after a series of studies conducted at the Western Electric Hawthorne plant in the early 20th century. The initial aim of the studies was to understand the impact of lighting levels on worker productivity. As expected, the first studies found that as lighting levels increased, so did productivity. However, researchers did a parallel experiment in which lighting levels were decreased, and found that productivity went up as the light decreased, even when lighting was

very low. After conducting a number of other related studies, the researchers concluded that productivity increases as a result of attention received by the workers. This phenomenon is believed to be due at least in part to the fact that work is a group activity, and employees strive for a sense of belonging (Hopp and Spearman, Factory Physics, 1996).

Volume 1, Number 2 - The P-K Formula (93 subscribers)

The Pollaczek-Khintchine (called P-K, for obvious reasons) formula gives the expected average WIP at a single-tool workstation where arrivals to the workstation are highly variable, and process times are somewhat less variable. More specifically, the formula applies when interarrival times to the workstation are exponentially distributed, and process times follow a general distribution (what is known as an M/G/1 queue). For tools that fit this description, the expected WIP can be easily computed from the mean interarrival time, the mean process time, and the variance of the process time distribution.

The P-K formula tells us that, if we look at individual tools in the fab, anything that we can do to reduce variability in the process times seen by successive lots will directly act to reduce WIP at these tools, without requiring a reduction in tool loading. And, as will be discussed in the next issue of the newsletter, cycle time will go down at the same time. The P-K formula is the mathematical justification for variability reduction efforts in a wafer fab.

Volume 1, Number 3 - Reducing Variability in Observed Process Times (119 subscribers)

Little's Law: The relationship between cycle time, WIP, and throughput.

The relationship between cycle time and WIP was first documented in 1961 by J. D. C. Little. Little's Law states that at a given throughput level, the ratio of WIP to cycle time equals throughput, as shown in the formulas below:

Throughput = WIP / Cycle Time
Cycle Time = WIP / Throughput

In other words, for a factory with constant throughput, WIP and cycle time are proportional. Keep in mind that Little's Law doesn't say that WIP and cycle time are independent of start rate. Little's Law just says if you have two of these three numbers, you should be able to solve for the remaining one. The tricky part is that cycle time and WIP are really functions of the start rate. So changing the start rate in fact changes all three parameters, but Little's Law should hold for the new numbers.

Volume 1, Number 4 - A Short Introduction To The Theory of Constraints (137 subscribers)

The Theory of Constraints is now in its fourth decade of development. In order to install any scheduling system into a complex job-shop environment (like a wafer fab), Eli Goldratt discovered that it may be necessary to first solve much deeper basic problems. It is this insight that led Goldratt to the concepts found in "The Goal", first published in 1984. Most people are introduced to the theory of constraints via "The Goal", often at the urging of a friend or colleague who has previously read it. The book is a fast-moving novel that considers the plight of Alex Rogo, a plant manager whose factory is in deep trouble.

The book outlines Alex's development (through the help of his mentor, Jonah) of a series of performance measures that, if improved, will result in the factory meeting its goal. To improve these performance measures requires a sequential process of identifying the bottleneck, improving the bottleneck's performance, and then identi-

fying the next bottleneck. Eventually, Alex's team learns that not all bottlenecks are physical tools in the factory, and that policy constraints can cause bottlenecks too. The book concludes with a systematic method for identifying and attacking system constraints (this is the theory of constraints, or TOC). FabTime's write-up on the subject concludes with some implications of TOC for wafer fabs.

Volume 1, Number 5 - Theory of Constraints and Just-in-Time Manufacturing (157 subscribers)

This article is concerned with an apparent conflict between an implication of the Theory of Constraints (TOC) as applied to wafer fabs and the application of just-in-time manufacturing (JIT). One implication of TOC is that utilization of manufacturing resources should be intentionally unbalanced. The result is an identifiable bottleneck that is managed to optimize the throughput-accounting performance measures (throughput dollars, operating expense, and inventory dollars).

Just-in-time manufacturing refers to the mindset spearheaded by Taiichi Ohno at Toyota Motor Company. In an effort that dates to the 1940's, the company developed and implemented a number of improvement techniques aimed at two basic goals:

1. Just-in-time delivery of material precisely when it is needed.
2. Autonomation, or machines that are both automated and fool-proofed.

JIT manufacturing techniques include setup reduction, total quality management, and kanbans. Kanbans in particular have developed a strong association with just-in-time manufacturing, which can cause considerable confusion, since kanbans require a more balanced line.

FabTime asks: Do the manufacturing recommendations of the theory of constraints (an unbalanced line being one of these) conflict with just-in-time manufacturing? We then reconcile Jonah's quote with Toyota's success by recognizing that both the theory of constraints and just-in-time manufacturing use WIP-limiting techniques - the difference lies in the extent to which these techniques are applied throughout the factory.

We conclude that if you are going to adopt a just-in-time manufacturing mindset, or a goal manufacturing mindset, you should set aside sufficient time to apply the entire process. Saving time by skipping to the answers (e.g. using existing implementation techniques such as kanbans or drum-buffer-rope) will likely result in little long-term gain.

Volume 1, Number 6 - Performance Measures Typically Used in Wafer Fabs (200 subscribers)

Wafer fabs cost a lot of money. Fab managers, therefore, are constantly under pressure to run them well, so that the huge investment in capital equipment is not wasted. But what does it mean to run a wafer fab "well"? In an ideal world, we would be able to keep all of that expensive equipment highly utilized, with the utilization dedicated completely to productive work. At the same time, we would have low and predictable cycle times, and a minimal amount of capital tied up in WIP. We would keep our operators busy and effective all of the time, so that we weren't wasting salary on having people stand around the fab. We would constantly improve our products, yet always maintain 100% line yield. We would keep costs down, but be able to charge high prices by having speedy time to market.

Of course this combination of circumstances is impossible for many reasons. A

wafer fab, as we discussed in the early issues of this newsletter, is a highly variable environment. In the presence of variability, high utilizations lead inevitably to high cycle time and WIP. You can load your operators and your tools heavily, or you can have low cycle time and WIP. You can't do both, unless you stamp out variability.

So the question is, what performance metrics should a fab manager use to make sure things are on track? And after deciding which to use, what are the correct definitions to use for these metric? We have observed, during our years of consulting, that different people often define the same metric differently. This is a source of confusion when comparing performance between or within companies. When people talk about utilization, for example, there are several things that they might mean. Similarly for turns. We therefore are proposing some definitions to apply within our niche of cycle time management. The terms defined in this article include starts, utilization, OEE, turns, throughput, line yield, cycle time, cycle time/raw process time, and cycle time per layer. We discuss each of these in detail.

Volume 1, Number 7 - Improving Factory Cycle Time Through Changes at Non-Bottleneck Tools (233 subscribers)

If you want to improve throughput for your fab, you need to start with the bottleneck (or bottlenecks), and work from there. However, this is not necessarily true when you're trying to reduce cycle time. We believe that you can reduce overall cycle time by reducing cycle time at any tool group in the factory.

The notion that you can improve overall cycle times by reducing cycle time at the bottleneck is obvious. And in fact, the bottleneck is a good place to start cycle time improvement efforts, since you probably have a large queue there, and lots of waiting time. The purpose of this article is to point out that you can ALSO reduce cycle time by making changes at non-bottleneck tools. This is far less obvious. With throughput, it doesn't matter if you process at a higher rate at non-bottleneck tools, because things get held up at the bottleneck anyway. Sometimes this happens with cycle time, too. But not always. We divide our discussion into three cases: tools located after the bottleneck in the process flow, tools located before the bottleneck, and tools located between visits to the bottleneck. We also include a series of concrete, low-cost suggestions for improving cycle time at non-bottleneck tools.

Our overall point is very simple: actions that you take to improve cycle time at non-bottleneck tools often improve overall product cycle times. For operations located before the first visit to the bottleneck, or after the last visit to the bottleneck, the cycle time reduction leads to an essentially direct reduction in the overall cycle time. For intermediate operations the situation is less clear, but we believe that improvements here can sometimes improve cycle time dramatically, and in the worst case, will not make cycle time any worse. If you focus your efforts strictly on bottleneck tools, then, you miss out on many opportunities for improvement.

Volume 1, Number 8 - Understanding the Impact of Single-Path Tools (258 subscribers)

Single-path tools are a common feature in wafer fabs. They occur whenever a single tool is the only piece of equipment qualified to process a particular operation. During fab startup, the majority of equipment will be single-path (since only one tool of each type has been purchased). As

fab volume grows, and duplicate tools are brought on-line, the number of single-path tools is usually reduced. At this point, however, there is often a choice in how the duplicate tools are configured -- cross-qualified in some fashion, or dedicated to individual operations.

In this article, we examine the impact of this tool-dedication decision on the number of single-path tools, and ultimately on cycle time, using concrete numerical examples and simple queueing approximations. Based on our analysis, the sample 100% dedicated-tool configuration results in an average cycle time that is nearly twice as long as the fully cross-qualified configuration. We also include a more intuitive explanation of the advantages of cross-qualification, based on other real-life examples.

While there are certainly other factors affecting the cross-qualification decision, our results suggest that if you do have a legitimate choice between cross-qualification and tool-dedication, you should consider the cycle time benefits of cross-qualification when making your decision.

Volume 2, Number 1 - Impact of Batch Size Decision Rules on Cycle Time (277 subscribers)

Batch tools are tools in which more than one lot may be processed at one time. They are generally used for very long operations, such as furnace bake operations. Processing time is usually independent of the number of lots in a batch, and once a batch process begins, it cannot be interrupted to allow other lots to join. From a local perspective, when a furnace is available and full loads are waiting, the decision to process a batch is obvious, since no advantage can be gained at that work area by waiting (although a decision may still be needed concerning which product type to process). However, when there is a furnace available and only partial loads of products are waiting, a decision must be made to either start a (partial) batch or wait for more products to arrive.

There are two problems with running a partial batch. One is that the unused capacity of the furnace will be "wasted." The other problem is that lots that arrive immediately after the batch starts cannot be added to the batch, and might have to wait many hours until another furnace is available. There are also problems that stem from waiting to form a full batch. The lots that are waiting to be processed incur extra queue time while waiting for other lots to arrive. The furnace is held idle, driving down its efficiency. And full batches contribute more to variability after the furnace operation.

This article discusses policies for deciding when to form a partial batch, using simple numerical examples and simulation results. We conclude that for batch tools that are not highly loaded, forcing full or near-full batches can significantly increase local cycle times, as well as overall fab cycle times.

Volume 2, Number 2 - Should You Reduce Lot Sizes to Reduce Cycle Times? (293 subscribers)

This article concerns possible changes to production lot sizes for cycle time improvement. For fabs running 50 wafer lots, changing to 24 or 25 wafer lots offers a potential cycle time reduction opportunity. However, there can be tremendous resistance to this idea, and there are a number of potential pitfalls. In this article, we first review the reasons for the cycle time reduction opportunity, and then discuss some of the pitfalls.

The justification of lot size reduction for cycle time reduction comes into play primarily due to time savings at per-wafer

tools, which can include critical tools such as steppers and implanters. In addition to providing these direct cycle time benefits, smaller lot sizes also make a fab more flexible, more adaptive in the event of problems, and can reduce variability. However, there are a number of issues to consider before changing the lot size, any one of which might keep a lot size reduction from being worthwhile, or even render it detrimental. These include capacity, material handling, MES, and dispatching/complexity issues, and are discussed in detail in the full article.

We have no black-and-white recommendation to make concerning lot sizes and cycle time. Smaller lot sizes may reduce cycle time, and make a fab more flexible. However, reducing the lot size can cause problems with material handling, capacity, MES performance, and fab complexity, particularly during the transition period. We suggest then, that you consider lot size reduction to reduce cycle times, but that you consider it very carefully.

Volume 2, Number 3 - Improving Cycle Time During a Downturn (317 subscribers)

Downturns are a fact of life in the cyclic semiconductor industry. Various factors contribute to their existence - capacity buildup (and the long lead-time required in capacity purchases), decline in selling prices, inventory build-up, and the general state of the economy. This one seems to have been triggered mainly by the last two factors, but explanations and predictions also seem to change every day.

The quickest way to reduce cycle time in a wafer fab is to significantly decrease start rates. This moves your factory to the left on the cycle time vs. factory loading curve, to a region of lower cycle times. The irony is that just when customers aren't clamoring for product, your fab can delivery product with record cycle time and on-time-delivery performance. It's very easy under these conditions to get a bit sloppy, and to take the lower cycle times for granted. But then when start rates begin to increase, when customers are paying attention again, your cycle times will degrade rapidly. If you don't have great cycle times now, you certainly won't have great cycle times when start rates go back up. Therefore, we suggest using this time to focus on low cost cycle time improvement efforts, including setup/dedication policy investigation, process analysis, layout analysis, bottleneck analysis, OEE/TPM analysis, simulation model validation, system upgrades, and education.

A downturn is a tough time - stressful, hard on your stock portfolio, and filled with the specter of layoffs. But it does offer at least one potential benefit: time to think. Time to think about manufacturing issues like lot size and batch size policies. Time to think about tool dedication schemes, and layout changes. Time to get your fab in order, and drive your cycle times to a minimum, before the next upturn comes along.

Volume 2, Number 4 - In-Depth Guide to OEE Resources (347 subscribers)

Most of our readers are familiar with the general concept of Overall Equipment Efficiency (OEE). OEE is a tool-level measure reflecting how much good product the tool produced relative to some theoretical amount that it could have produced. Typical OEE values in a wafer fab are less than 50%. Given the high cost of equipment, there is a clear incentive to make OEEs as high as possible. OEE is the measurement that's used in TPM (Total Productive Maintenance), a methodology for improving the entire manufacturing process.

In this article, we review the formulas for

calculating OEE (both the full formula and a short-cut version), as well as some of the reasons for low OEE in wafer fabs. We also include a series of links to OEE resources on the Internet (including primary resources from SEMI and SEMATECH), as well as some additional published OEE references.

The power of OEE is that it provides a clearly defined metric by which equipment performance improvement projects can be measured. SEMI and SEMATECH have gone to great lengths to define OEE, and also the necessary supporting metrics like the SEMI E-10 equipment states. The nice thing about this is that it means that you can compare OEE values across factories, and even across companies, and get a true picture of your factory's performance. Another nice thing about OEE is that it drives you to do good things, like reduce setup and rework and scrap and starvations due to WIP or operator shortages. By focusing on the six types of losses highlighted by OEE, you can design a strong equipment improvement program, and monitor your progress through trends in the overall metric.

Community News/Announcements

Job Change Announcement - Todd Hudson:

Todd Hudson has taken a job as the Operations Director at Planar Systems, a flat panel display manufacturer (www.planar.com). He will be responsible for running two factories in Oregon. Previously, Todd was Head Maverick and founder of The Maverick Group, LLC, an industrial engineering and operations research firm (www.themavgroup.com). Todd has more than 20 years' experience working with companies in industries such as microelectronics, information technology, automotive and light manufacturing.

Samsung A Finalist for O.R. Prize (from an announcement distributed by Professor Robert Leachman)

"Samsung Electronics Corporation's sophisticated use of scheduling systems while defying a downturn for semiconductor manufacturers resulted in its selection as a runner-up in the Franz Edelman Competition for Achievement in Operations Research and the Management Sciences at the Hyatt Regency La Jolla today (May 22, 2001). The Institute for Operations Research and the Management Sciences (INFORMS®) presented the award for its project entitled "SLIM: Short Cycle Time and Low Inventory in Manufacturing."

"The operations research models used by Samsung allowed it to increase manufacturing efficiency while the DRAM industry as a whole was in trouble," said Donald R. Smith of Lucent Technologies, chair of the award committee.

SLIM is a set of scheduling systems that manages the product flow times in semiconductor manufacturing. Since 1996, Samsung has progressively applied SLIM at its worldwide semiconductor manufacturing facilities. The system features automated on-line scheduling of the entire semiconductor manufacturing process, as well as off-line applications in planning target cycle times, output schedules, and qualifications and additions of processing equipment.

The cycle time to fabricate dynamic random access memory (DRAM) devices was reduced from 80 to 30 days. Competing in a volatile industry that sees falling

prices and increasing demands for prompt delivery, SLIM gave Samsung a sales revenue gain of more than $1 billion dollars over the period 1996-2000, when other DRAM manufacturers were experiencing serious losses.

The team included - Leachman & Associates: Robert C. Leachman, Jeenyoung Kang, Vincent Lin; and Samsung Electronics Co., Ltd.: Jae-Wook Kim, Young-In Kim. The six finalists for the award, all of whom are recognized by the prize committee, are U.S. Army Recruiting; NBC; The Jan de Wit Lírios Company, Brazil; OnStar; Samsung; and the first-prize winner, Merrill Lynch U.S. Private Client Group. Additional information about the contestants is online at http://www.informs.org/Press/SanDiego02.htm. The competition was held at a new INFORMS conference, "Optimizing the Extended Enterprise in the New Economy."

This is the 30th year that the prestigious $15,000 competition has been held. The award is jointly sponsored by INFORMS and CPMS, the Practice Section of INFORMS. The INFORMS Edelman Award recognizes outstanding implemented work that has had a significant, positive impact on the performance of the client organization."

SEMICON West - July 16-20, 2001

SEMICON West is coming up soon. You can pre-register online (there is no charge if you pre-register) at www.semi.org/web/wexpositions.nsf/url/01westhome. The Wafer Processing segment of the show will be held July 16-18 at the San Francisco Moscone Center. The Final Manufacturing segment will be held July 18-20 at the San Jose Convention Center. SEMICON West is "the world's largest international tradeshow and conference dedicated to semiconductor equipment, materials, suppliers and services." We hope to see you there.

FabTime welcomes the opportunity to publish announcements for individuals or companies. Simply send them to Jennifer.Robinson@FabTime.com.

FabTime Recommendations

FabTime's new book of the month for June is "How We Know What Isn't So" by Thomas Gilovich (www.fabtime.com/howweknow.htm). This book discusses areas in our everyday lives in which our intuition fools us, such as our reliance on the idea of "streaks" in sports.

Book Links: FabTime has recently added direct links to individual book pages on Amazon for all of our reviewed books (www.fabtime.com/books.htm). This gives you single-click access to the books, so that if you find any of them interesting, you can order them for yourself more easily. So far we have reviewed the following books:

- Focus! by Al Ries (www.fabtime.com/focus.htm)
- The Goal by Eli Goldratt and Jeff Cox (www.fabtime.com/goal.htm)
- Factory Physics by Wallace Hopp and Mark Spearman (www.fabtime.com/physics.htm)
- Crossing the Chasm by Geoffrey Moore (www.fabtime.com/chasm.htm)
- Creating a Customer-Centered Culture by Robin Lawton (www.fabtime.com/customer-ctr.htm)
- Microchip Fabrication by Peter Van Zant (www.fabtime.com/microchip.htm)
- The Effective Executive by Peter Drucker (www.fabtime.com/effective.htm)

- World Class Manufacturing Casebook by Richard Schonberger (www.fabtime.com/worldclass.htm)
- The Theory of Constraints and Its Implications for Management Accounting by Eric Noreen, Debra Smith, and James MacKey (www.fabtime.com/tocacct.htm)
- The Tipping Point by Malcolm Gladwell (www.fabtime.com/tippingpoint.htm)
- The Non-Designer's Design Book by Robin Williams (www.fabtime.com/designer.htm)
- Root Cause Analysis by Robert Latino and Kenneth Latino (www.fabtime.com/rootcause.htm)
- Faster by James Gleick (www.fabtime.com/faster.htm)
- Necessary But Not Sufficient by Eli Goldratt, Eli Schragenheim, and Carol Ptak (www.fabtime.com/necessary.htm)
- Why Systems Fail And How to Make Sure Yours Doesn't by David Turbide (www.fabtime.com/systems.htm)
- Leading with the Heart by Mike Krzyzewski and Donald Phillips (www.fabtime.com/CoachK.htm)

Of these books, Factory Physics is the one that has received the most positive feedback from our readers. We also consider The Goal, The Effective Executive, The Non-Designer's Design Book, and Focus! to be essential reading for everyone in business. The Goal helps in understanding manufacturing, the Effective Executive is useful for time management and prioritizing work, The Non-Designer's Design book helps in creating documents for presentation to others, and Focus! tells how to succeed in the long-term through focusing your efforts.

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