FabTime Cycle Time Management Newsletter

Volume 3, No. 2 February 2002

Information

Mission: To discuss issues relating to proactive wafer fab cycle time management.

Publisher: FabTime Inc. FabTime sells cycle time management software for wafer fab managers.

Editor: Jennifer Robinson

Contributors: John Fowler (ASU)

Table of Contents

- Welcome
- Community News/Announcements
- Subscriber Discussion Forum
- Main Topic Cycle Time and Hot Lots
- Recommendations and Resources
- Current Subscribers

Welcome

Welcome to Volume 3, Number 2 of the FabTime Cycle Time Management Newsletter. The newsletter now has well over 700 subscribers, with the number increasing almost every day. I've been especially pleased to see that the amount of subscriber discussion has been increasing as well, although the amount of feedback is down slightly in this particular issue. So I'm making a request to you, our readers: if you have a question about fab cycle time or performance improvement, or if you have thoughts on someone else's previously included question, please write to me and let me know. Your question/response can be attributed to you, or included anonymously, as you prefer. Either way, I think that this type of discussion makes the newsletter more valuable for all of us. And I would like to once again thank all of the people to date who have contributed, with special thanks to our top repeat contributors, John Fowler, Bob Kotcher, Scott Mason, V. A. Ames, and Walt Trybula.

This month we are pleased to highlight a new sales and implementation partnership that we have established with Abbie Gregg, Inc., a Phoenix-based engineering and consulting firm. FabTime's other sales partners include Durham ATS Group, James Nagel Associates, MTE Associates, Productivity Partners Ltd, and SemiTorr NorthWest, Inc. This month's main topic concerns cycle time and hot lots. The article is drawn from a presentation that Frank Chance made at Arizona State last month. We present a formula for estimating the average cycle time of lots through a tool that processes lots with different priorities (regular lots and hot lots). We provide a numerical example that shows how the cycle time of the regular lots increases as the percentage of hot lots is increased, and discuss implications for managing hot lots in a wafer fab.

Thanks for reading! -- Jennifer

Fablime

325M Sharon Park Dr. #219 Menio Park CA 94025 Tel: 408 549 9932 Fax: 408 549 9941 www.FabTime.com

Community News/Announcements

FabTime Announces Sales and Implementation Partnership with Abbie Gregg, Inc.

Menlo Park, CA. February 19, 2002 -FabTime Inc. today announced that it had established a sales and implementation partnership with Abbie Gregg, Inc. (AGI). AGI provides engineering and consulting services for the semiconductor, flat panel display and other microelectronics industries. AGI will assist in making FabTime wafer fab cycle time management software sales, particularly in AGI's local area of Arizona and New Mexico, and will offer engineering support during FabTime implementation projects.

"This partnership with AGI is a great opportunity for FabTime," said Frank Chance, President of FabTime. "Having AGI's assistance on sales and implementation projects will allow us to focus more on our core strength, software development."

"We look forward to working with FabTime," said Abbie Gregg, President of AGI. "We think that their software can help our clients to improve their fab performance. It is great for looking at key indicators such as moves and WIP turns, and drilling down to find the root causes of cycle time." Corporate customers for FabTime's cycle time management software include Advanced Micro Devices (NYSE: AMD) and Headway Technologies, a division of TDK (NYSE: TDK). A form for requesting more information about the software is available at www.fabtime.com/ software.htm.

About Abbie Gregg, Inc.

Founded in 1985, Abbie Gregg, Inc. (AGI) has provided technical expertise to the rapidly growing microelectronics industry for over a decade. AGI's services include process engineering, yield enhancement, cleanroom design, technical training, factory/cost modeling, detailed planning, and facility start-up. AGI's clients have included: Amkor (NASDAQ: AMKR), FlipChip Technologies, Eastman Kodak (NYSE: EK), Philips Semiconductors, Motorola (NYSE: MOT), Ericsson Components, Texas Instruments (NYSE: TXN), White Oak Semiconductor, LSI Logic (NYSE: LSI), AMD, HP (NYSE: HWP), Kopin Corporation (NASDAQ: KOPN), and GMT Microelectronics. AGI's website is located at www.abbiegregg.com.

FabTime welcomes the opportunity to publish community news and announcements. Simply send them to Jennifer.Robinson@FabTime.com.

Subscriber Discussion Forum

Performance Indices - The Human Dimension

Last month, Sihar Snir asked "what are the most widely used Performance Measures in the industry regarding Human Resource to Activity relations?" One of our subscribers sent in the following response. "One of the best measurements on this is total SNE (salaried nonexempt) employees in the wafer fab per number of wafers aligned. This measurement is a good normalized value for both logic and memory producers. We have used

FabTime

Cycle Time Management Newsletter

this at our company when benchmarking with other semi manufacturers. The total SNE number needs to include all persons both in the fab and in support groups. This is not a perfect number, but it is usually quick to calculate and compare for benchmarking purposes."

Cycle Time Reduction Case Studies

Another subscriber wrote: "I am searching for "case study" articles on production/ manufacturing cycle time reductions. I have proceeded to implement a method within our process - however I am interested in what other companies have done attempting to go about measuring such a complex topic. Would you be so kind as to send me some information pertaining to "case study" articles? Any help you can provide in this matter would be greatly appreciated."

FabTime Response:

For several years I (Jennifer) have maintained a bibliography on capacity and cycle time analysis for wafer fabs. The bibliography can be found on my personal website, at www.jkrconsult.com/capbib.htm. Section 17: Lead Times and Section 24: Performance Evaluation both contain many cycle time reduction case study references. Some of these can also be found on FabTime's website, at www.FabTime.com/CTBiblio.htm. Abstracts to most of the articles are available upon request. And if any other readers know of cycle time reduction case studies that we are missing, please let us know so that we can add them to the list.

Production Equipment Efficiency

John Fowler (ASU) added an excellent point to our discussion on PEE. He wrote: "One additional thing that might be said about PEE is that it is a good indicator of the amount of variability that a tool introduces into the factory. A high PEE means that lots don't often get held up because bad things are happening at the tool, while a low PEE means the opposite."

Cycle Time and Hot Lots

Introduction

Do you run hot lots in your fab? Our guess is that you do. Hot lots seem to be an inevitable fact of life when managing a wafer fab. They are often needed because of demands from specific high-priority customers, or for engineering or time to market reasons (e.g. you have to get this lot through to get to the next stage in the development cycle, so that you can release the product to market before your competitor's product). Hot lots serve a useful purpose. You can usually get a few lots out quickly without great disruption to your fab. Reducing the cycle time of all lots in the fab to the same levels would require a huge project, if it could be done at all. However, hot lots are a problem, too. They increase variability in the fab and increase the cycle time of regular (non-hot) lots. And the more hot lots you have, the less effective they are, because they start interfering with one another.

FabTime

Cycle Time Management Newsletter In this article, we will present a formula for estimating the impact of hot lots on regular lot cycle times, and discuss the implications on this formula on managing hot lots.

Estimating the Cycle Time of a Single Machine

Let's start with the simplest case. Assume that we have a single tool, with highly variable times between arrivals, highly variable process times (where by highly variable we mean exponentially distributed), and no downtime events. This is called an M/M/1 system in queueing terminology. For an M/M/1 system, the average cycle time of lots processed is a function of arrival rate and processing rate, as follows. Let

lambda = arrival rate to the tool (e.g. lots/ hour); and

mu = processing rate of the tool (e.g. lots/ hour) (assume that mu is independent of lot size for this tool)

then

rho = lambda / mu = utilization (or traffic intensity)

and

Cycle Time = [(rho/mu) / (1 - rho)] + [1/mu]

where

 $[(\rm rho/mu)~/~(1$ - rho)] is the average queue time

and

[1/mu] is the average process time.

For example, let:

lambda = 10 lots/hour

$$mu = 12 lots/hour$$

then

rho = lambda/mu = 10/12 = 0.8333

and

Cycle Time = [(rho/mu) / (1 - rho)] + [1/mu] = [(.8333/12) / (1 - .8333)] + [1/12]

= [.06944/.1667] + .08333 = .41667hours + .0833 hours = 0.50 hours = 25 minutes + 5 minutes = 30 minutes.

So, the machine can process 12 lots per hour, requiring an average of five minutes to process each lot. However, because the tool is relatively highly loaded at 83%, lots wait an average of 25 minutes each before being processed. This formula can easily be coded into a spreadsheet and used to show how queue time, and hence cycle time, increases as lambda approaches mu. Note that we applied this formula for perlot arrival rate and per-lot arrival time. It can also be applied on a per-wafer basis (for example, if process time varies according to the number of wafers in the lot).

Including Priority Classes

Now suppose we have almost the same system as above, except that there are two priority classes of lots. High priority lots are always processed ahead of low priority lots, although lots already in process are never interrupted. High priority lots just move to the front of the line as soon as they arrive. Let

lambda_H = high priority lot arrival rate to the tool (e.g. lots/hour)

mu_H = high priority processing rate of the tool (e.g. lots/hour) (assume that mu is independent of lot size for this tool)

lambda_L = low priority lot arrival rate to

Fablime

Cycle Time Management Newsletter

the tool (e.g. lots/hour)

 $mu_L = low priority processing rate of the tool (e.g. lots/hour) (assume that mu is independent of lot size for this tool)$

then

rho_H = lambda_H / mu_H rho_L = lambda_L / mu_L

and

nu (intermediate term) = (rho_L / mu_L) + (rho_H / mu_H)

CT_H = high priority cycle time = [nu / (1 - rho_H)] + [1/ mu_H]

 $CT_L = low priority cycle time = [nu / (1 - rho_H)(1 - rho_H - rho_L)] + [1/mu_L]$

For example, suppose that 10% of the lots in the previous example are converted to hot lots.

Then lambda_H = 1 lot/hour, lambda_L = 9 lots/hour, and mu_H = mu_L = 12 lots/hour.

rho_H = 1 / 12 = .08333 rho_L = 9/12 = .75

and

nu = (.0833/12) + (.75/12) = .06944

 $CT_H = [.06944 / (1 - .0833)] + [1/12] =$.0758 + .08333 = .15909 hours = 4.545 min + 5 min = 9.545 min

 $CT_L = [.06944 / (1 - .0833)(1 - .0833 - .75)] + [1/12] = .4545 + .0833 = .5379$ hours = 27.27 min + 5 min = 32.27 min

Comparing this to the previous example, we see that if we make 10% of the lots hot, we can get the hot lots through in less than 10 minutes each, while increasing the regular lot cycle time by 2.27 minutes, on average. Perhaps an acceptable trade-off. But what if we have a larger percentage of hot lots.

% Hot	CT_H (min.)	CT_L (min.)	Wt. Avg CT (min.)
10	9.55	32.27	30.0
20	10.00	35.00	30.0
30	10.56	38.33	30.0
40	11.25	42.50	30.0
50	12.14	47.86	30.0

That is, the more hot lots we have, the higher the cycle times are for both regular and hot lots. With 50% hot lots, the cycle time of the regular lots is increased by more than 50%.

Note, however that weighted average cycle time is conserved. That is:

(lambda_H * CT_H + lambda_L * CT_L) / (lambda_H + lambda_L)

stays constant at 30 minutes. This means that cycle time is not being created out of thin air by hot lots -- it is simply being reallocated between the hot lots and the regular lots. If we have a small percentage of hot lots, we are scooping the cycle time off the backs of those lots and spreading it across the much larger percentage of regular lots, and thus the increase in regular lot cycle time is not very large. But as we increase the proportion of hot lots, this decreases the number of regular lots that are left to shoulder the cycle time burden, and increases the inflation of regular lot cycle time. This is shown in the figure at the top of the next page.

Implications of Priority Class Formula

Comparing the formula for regular lot cycle time (in the presence of hot lots) with the original formula for cycle time (without priorities), we can see that the hot lots inflate the regular lot cycle time by a factor

FabTime

Cycle Time Management Newsletter



Cycle Time vs. Hot Lot Percentage

approximately equal to (1 / (1-rho_H)). When rho_H is very small (as in the example with 10% hot lots), the inflation is small. But when rho_H becomes large, the inflation can be quite significant. In practice, most fabs do keep the percentage of hot lots low, thus deriving the benefit of getting a few lots out quickly, without significantly inflating the cycle time of the other lots.

Do Hot Lots CREATE Cycle Time?

We saw from the example above that weighted average cycle time is conserved in the presence of hot lots. That is, in the simple world modeled above, hot lots do not create extra cycle time. Rather, they cause cycle time to be re-allocated between hot lots and regular lots. However, in the real world, we believe that hot lots do create extra cycle time, through some combination of the following mechanisms:

FabTime

Cycle Time Management Newsletter

Volume 3, No. 2

■ Breaking setups for hot lots increases the number of required setups, which increases variability and decreases standby time. ■ Holding tools idle for hand-carried hot lots decreases available standby time.

■ Tool dedication for hot lots, even if warranted in terms of capacity, reduces the number of parallel servers available for regular lots. (We will examine the relationship between tool dedication and cycle time in an upcoming newsletter).

Taken together, the mechanisms listed above mean that cycle time for regular lots will likely be inflated by more than the (1 / (1-rho_H)) factor listed above. As a rule of thumb, then, it is probably safer to use this factor as a best case estimate of the impact of hot lots, and to assume that regular lot cycle time will be inflated by at least this amount.

Conclusions

This article introduced a simple formula for estimating cycle time through a single tool in the presence of two priority classes. Clearly, the formula is an oversimplification of the situation in a wafer fab. However, we believe that the formula can be used to get a rough idea of the impact of hot lots on a single tool, and that the general conclusions regarding the impact of hot lots do apply to the fab as a whole. We have previously done simulation studies using wafer fab models that have given similar results. In those studies, up to about 10% hot lots the regular lot cycle time increased only slightly. However, the impact on regular lot cycle time increased steadily (and non-linearly) as the percentage of hot lots was increased. These results can be extended to look at multiple classes of hot lots.

Closing Questions for FabTime Subscribers

■ How do you manage hot lots, to keep them from excessively impacting regular lot cycle time?

■ Do you set a percentage?

Do you set a maximum total number of hot lots?

■ Is there some numeric criterion used, or is it just the fab manager's gut feeling?

If any readers would care to address these questions, we will print your remarks (anonymously or attributed, as you wish) in the next issue. Send your responses to Jennifer.Robinson@FabTime.com.

References

Some other studies on hot lots in wafer fabs include:

■ A. M. Bonvik, "Estimating the Lead Time Distribution of Priority Lots in a Semiconductor Factory," Working Paper from Operations Research Center, Massachusetts Institute of Technology, 1-26, 1994.

B. Ehteshami, R. G. Petrakian, and P. M. Shabe, "Trade-Offs in Cycle Time Management: Hot Lots," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 5, No. 2, 101-105, 1992.

■ D. Fronckowiak, A. Peikert, and K. Nishinohara, "Using Discrete Event Simulation to Analyze the Impact of Job Priorities on Cycle Time in Semiconductor Manufacturing," *Proceedings of the 1996 Advanced Semiconductor Manufacturing Conference and Workshop (ASMC 96)*, Boston, MA, 151-155, 1996.

■ Y. Narahari and L. M. Khan, "Modeling the Effect of Hot Lots in Semiconductor Manufacturing Systems," *IEEE Transactions on Semiconductor Manufacturing*, Vol. 10, No. 1,185-188, 1997.

■ Casey O'Connor and Liyu Yang, "Hot Lots." Web article located at http:// www.glue.umd.edu/~cjpo/Hotlot.html, dated 12/31/99.

■ W. J. Trybula, "Hot Jobs, Bane or Boon," *Proceedings of the 1993 IEEE/ CHMT International Electronics Manufacturing Technology Symposium*, Santa Clara, CA, 317-322, 1993. Also available as SEMATECH Technology Transfer No. 93041617A-ER.

The abstracts to the above are available from FabTime upon request. All of the studies document the effect that hot lots have on regular lot cycle times. Both D. Fronckowiak, A. Peikert, and K. Nishinohara's paper and Trybula's paper suggest, as we do, setting an upper bound on the number of hot lots, to minimize the effect on regular lot cycle times.

For queueing formulas on priority queues, we used:

■ N. Prabhu. 1981. Basic Queueing Theory. Technical Report No. 478, School of Operations Research and Industrial Engineering, Cornell University, Ithaca, New York.

■ S. M. Ross, *Introduction to Probability Models: Fourth Edition.* Academic Press, Harcourt Brace Jovanovich: San Diego, CA, 1989.

FabTime

Cycle Time Management Newsletter

FabTime Recommendations

Extra Non-Bottleneck Capacity Article

We are recommending this article as it relates to our previous issues on including cycle time in the capacity planning process, and on cycle time reduction at non-bottleneck tools.

J. W. Patterson, L. D. Fredendall, C. W. Craighead, "The Impact of Non-Bottleneck Variation in a Manufacturing Cell," *Production Planning and Control*, Vol. 13, No. 1, 2002, 76-85.

Abstract: Protective capacity is the 'extra' capacity placed at non-bottleneck resources to absorb random disruptions in planned levels of performance so that the bottleneck resource continues to be effectively utilized. A full factorial experiment with a simulation model was conducted to explore issues associated with the quantity and location of processing variance in a five-station manufacturing cell. The cell's performance was measured using both mean flow time (MFT) and bottleneck shiftiness (SHIFT) for 3 patterns of variance for the non-bottlenecks at 5 different levels of variation. In order to investigate the importance of the quantity of added capacity on the variation both a low level of protective capacity (10%) and a high level (50%) were considered. The results indicate that having the higher variation work centres close to the bottleneck provides reduced MFT and SHIFT. The performance measures improved at both the low and high setting of protective capacity.

Printed Circuit Board Assembly References

Yves Crama, Joris van de Klundert, and Frits Spieksma maintain an annotated bibliography of material related to PCB assembly at www.math.unimaas.nl/personal/fritss/bibliography/bibliogr.htm. The bibliography includes journal publications, theses, conferences proceedings, and working papers. They don't guarantee that the bibliography is comprehensive, but we suggest that it's a good place to start if you are looking for references on PCB assembly.

Snaglt Screen Capture Software

SnagIt is a handy little program that lets you capture screen snapshots and save them in various graphics formats. You can specify which portion of the screen to capture (unlike the standard PrintScreen command), or set the program to capture the active window or full screen by default. You can save files to the standard graphics formats, and then insert them easily into documents or web pages. We use it for preparing our software training materials and for developing marketing materials. It offers considerable flexibility over the standard Windows tools, worth the \$39.95 single user price if you work with many screen snapshots. You can download SnagIt from the TechSmith website, at www.techsmith.com. There is a 30 day free trial - after that you must pay for a license.

FabTime

Cycle Time Management Newsletter

Subscriber List

Total Subscribers: 730 1st Silicon (1) 3M Company (2) Abbie Gregg Inc. (2) ABB Semiconductors (3) Adexa Corporation (1) Advanced Micro Devices (38) Affymetrix (1) Agere Systems (5) Agilent Technologies (4) Aisin Indonesia (1) Alfalight Canada (1) Alpha Industries (1) Alpha-Sang (1) AMI Semiconductor (2) Amkor (3)AMR Research (1) Analog Devices (5) Applied Materials Corporation (10) Aralight Corporation (2) Arch Wireless (1) Arizona State University (5) Arkansas Tech University (1) Asia Management Group (1) ASM International NV (1) ASML (3) ATMEL (4) Axsun Technologies (1) Bookham Technology Plc (1) Boston Scientific (1) Bovis Lend Lease Microelectronics (1) BP Solar (3) Brooks Automation (2) Byelorussian State Economic Univ. (1) Cabot Microelectronics Ltd. (1) California Polytechnic State University (1) C&D Aerospace (1) Cannon Precision (1) Canon USA (1) Carsem M Sdn Bhd (3) Chartered Semiconductor Mfg (23) ChipPAC, Inc. (1) CMC Electronics (1) Compugraphics International Ltd. (1) Conexant Systems, Inc. (4) Continental Device India Ltd. (1)

Cornell University (1) Corning (1)Cox High Speed Internet (1) C-Port Corporation (1) Cree, Inc. (1) Cronos Integrated Microsystems (1) Cummins S. de R.L. de C.V. (1) Cyberfab (1) Dallas Semiconductor (2) Datacon Semiconductor Equipment GmbH (1) Delta Design (1) Dick Williams and Associates (1) DomainLogix Corporation (1) Dominion Semiconductor (5) Dow Corning Corporation (1) Durham ATS Group (4) Dwarkadas Associates (1) Eastman Kodak Company (3) Electroglas, Inc. - Statware Division (2) e-METS Co, Ltd (1) Ernst & Young (1) eSilicon Corporation (2) Eskay Corporation (1) FabTime (3) Fairchild Imaging (1) Fairchild Semiconductor (3) Fort Dearborn Company (1) Fraunhofer IPA (1) Fujitsu Microelectronics, Inc. (1) General Semiconductor (2) Headway Technologies (2) Hewlett-Packard Company (6) Hitachi, Ltd. (1) Hitachi Nippon Steel Semiconductor (4) Huck Fasteners (1) Hynix Semiconductor Mfg America Inc. (1) IBM (9) ICG / Semiconductor FabTech (1) IDC(7)IMEC (2) Infineon Technologies (33) Infosim Networking Solutions (1) INSEAD (3) Institut National Polytechnique de Grenoble (2) Integrated Device Technologies (2) Integrated Technologies Company (2)

FabTime

Cycle Time Management Newsletter

FabTime

Cycle Time Management Newsletter

Volume 3, No. 2

Intel Corporation (33) Intelligent Quality Systems (1) International Rectifier / HEXAM (2) Intersil (3) Interstar Technology (1) Jacobs Consultancy (1) James Nagel Associates (1) JDS Uniphase (3) Johnstech International Corp. (1) Kansas State University (1) Ken Rich Associates (1) KLA-Tencor (1) Kulicke & Soffa Industries, Inc. - K&S (2) Kymata - Alcatel (1) Lexmark International, Inc. (1) Linear Technology (1) Litel Instruments (1) LSI Logic (8) Lynx Photonic Networks (1) Macronix International Co. (5) Managed Outsourcing, Inc. (2) MASA Group (1) Maxim Integrated Products, Inc. (3) Maxtor (1)MECA Electronics, Inc. (1) Medtronic (5) MEMS Optical (1) Methode Electronics, Inc, (1) Metrology Perspectives Group (1) Micrel Semiconductor (2) Microchip Technology (1) Micron Technology, Inc. (1) Micro Photonix Int. (1) MicroVision-Engineering GmbH (1) Motorola Corporation (41) MTE Associates (1) Nanometrics (2) Nanyang Technological University (4) National Chiao Tung University (1) National Semiconductor (10) National University of Ireland (1) National University of Singapore (2) NEC Electronics (6) Nortel Networks (6) Ohio State University (1) Oklahoma State University (1) ON Semiconductor (8)

Onix Microsystems (1)

Palmborg Associates, Inc. (2) Pelita Harapan University (1) Penn State University (1) Peter Wolters CMP Systeme (1) Philips (16) Piezo Technology Inc. (1) Planar Systems (2) PolarFab (3) Politecnico of Milano (1) Powerex, Inc. (3) PRI Automation (2) Productivity Partners Ltd (1) ProMOS Tech. (1) Propsys Brightriver (1) PSI Technologies, Inc. (1) Quanta Display Inc. (1) Ramsey Associates (1) Raytheon (1) Read-Rite Corporation (2) Redicon Metal (1) Rexam (1) Rockwell Automation (1) RTRON Corporation (2) SAMES (1) Samsung (5) Saint-Gobain Company (1) Seagate Technology (17) SEMATECH (16) Semiconductor Research Corp. (1) SemiTorr NorthWest, Inc. (1) Serus Corporation (1) SEZ America, Inc. (1) Shanghai Grace Semiconductor Mfg. (1) SiGen Corporation (1) Silicon Manufacturing Partners (4) Silterra Malaysia Sdn. Bhd. (5) Sipex Corporation (1) Sony Semiconductor (1) SoundView Technology (3) SSMC (1) STMicroelectronics (27) Stonelake Ltd. (1) Storage Technology de Puerto Rico (1) Superconductor Technologies, Inc. (1) Süss MicroTec AG (1) Synergistic Applications, Inc. (1) Synquest (2) Takvorian Consulting (1)

TDK (1) TECH Semiconductor Singapore (21) Terosil, a.s. (1) Texas A&M University (1) Texas Instruments (12) Tokyo Electron Deutschland GmbH (1) Tower Semiconductor Ltd. (1) Triniti Corporation (1) TriQuint Semiconductor (3) Tru-Si Technologies (1) **TRW** (1) TSMC (3) UMC (6) Unisem (1) United Monolithic Semiconductors (1) Unitopia Taiwan Corporation (2) University of Arkansas (1) University of California - Berkeley (4) University of Mining and Metalurgy -Poland (1) University Porto (1) University of Texas at Austin (1) University of Virginia (1) University of Wuerzburg - Germany (1) Velocium (1) Virginia Tech (3) Vitesse Semiconductor (1) Wacker Siltronic (4) WaferTech (10) Win Semiconductor (1) Wright Williams & Kelly (8) Xerox Brazil (1) X-FAB Texas, Inc. (3) Yonsei University (1) Zarlink Semiconductor (4) Zetek PLC (1) Unlisted Companies (13)

Consultants:

Carrie Beam Vinay Binjrajka (PWC) Javier Bonal Steven Brown Stuart Carr Alison Cohen Paul Czarnocki Scott Erjavic Greg Fernandez Ted Forsman Navi Grewal Corv Hanosh Norbie Lavigne Michael Ray Bill Parr Nagaraja Jagannadha Rao Lyle Rusanowski Mark Spearman (Factory Physics, Inc.) Dan Theodore Craig Volonoski

Note: Inclusion in the subscriber profile for this newsletter indicates an interest, on the part of individual subscribers, in cycle time management. It does not imply any endorsement of FabTime or its products by any individual or his or her company. To protect the privacy of our subscribers, email addresses are not printed in the newsletter. If you wish contact the subscribers from a particular company directly, simply email your request to the editor at Jennifer.Robinson@FabTime.com. To subscribe to the newsletter, send email to the same address. You can also subscribe online at www.FabTime.com/ newsletter.htm. We will not, under any circumstances, give your personal information to anyone outside of FabTime.



Cycle Time Management Newsletter