FabTime Cycle Time Management Newsletter

Volume 3, No. 5 May 2002

Information

Mission: To discuss issues relating to proactive wafer fab cycle time management.

Publisher: FabTime Inc. FabTime sells cycle time management software for wafer fab managers.

Editor: Jennifer Robinson

Table of Contents

Contributors: Abbie Gregg (AGI); Juan Manuel Torres (Seagate); Roger Watson (jTask); Robert Hood (WaferTech); and Ken Beller

Welcome

Welcome to Volume 3, Number 5 of the FabTime Cycle Time Management Newsletter. Frank and I enjoyed having the opportunity to meet a number of newsletter subscribers in person at the SEMICON Europa and MASM conferences last month. We hope we'll be able to meet more of you in the future.

In this issue, we have several industry announcements, including a job availability notice from Seagate, and subscriber questions related to wafer starts methodologies, product costing, operator planning, ramp planning, and mean time between assists. We think that many of these issues are positive indicators of industry improvement. Regarding the subscriber discussion forum itself, we've noticed that fewer people are writing in response to one another's questions, and fewer people who submit questions are willing to have their name included in the discussion. I'm not sure why this is - perhaps a consequence of the subscriber list becoming larger - but I'll just point out that you, the subscribers, will make this forum more valuable if you take the time to share ideas with each other.

Our main article this month is about quantifying the bottom-line benefits of cycle time improvement. We discussed one particular benefit in a previous newsletter issue. In this new article, we provide a more comprehensive framework for linking cycle time management to financial returns. An Excel spreadsheet tool for what-if analysis is provided on FabTime's website. There's both money to be saved and additional revenue to be earned through cycle time improvement. Under the assumptions in our default example, the total annual benefit of cycle time improvement could be more than half a million dollars.

Thanks for reading! -- Jennifer

FabTime

325M Sharon Park Dr. #219
Menlo Park CA 94025
Tel: 408 549 9932
Fax: 408 549 9941
www.FabTime.com

Community News/Announcements

AGI Booth Announcement - SEMICON

FabTime received this announcement from our Arizona and New Mexico sales and implementation partner - AGI. "We are looking forward to seeing you at Semicon West 2002! AGI, Abbie Gregg, Inc. will be exhibiting at Booth 2445, at the far end of the main floor (away from entrance), on the right-hand side of the South Hall in the Moscone Center.

See our latest Facility Planning and Industrial Engineering Software: JupiterC, IoC, FabTechC, and eValuateC. See updates on our latest Fab Renovation, Greenfield Site and Yield Enhancement Projects. Get info on our latest training classes, including: "This Old Fab!!" and "Cleanroom Design/Build Short Course" with Arizona State University. Hear about our latest domestic and international projects including R&D and Production in Silicon Wafers (300mm), GaAs, InP, Laser Diodes, MEMS, BioChip, and other novel materials. Hear about state of the art Imaging and Metrology Room designs. We now complement our IE and Process Engineering Services with A&E Design/Build and Tool Hook-up Support.

For more information, visit our website at www.abbiegregg.com, or Contact Abbie Gregg, President at agregg@abbiegregg.com. Call us at (480) 446-8000. See you in San Francisco!"

Note that FabTime's Frank Chance and Jennifer Robinson will also be attending SEMICON. Please contact us if you would like to arrange a FabTime software demo.

Job Availability Notice - Seagate

Position Summary: Seagate's Recording Head operation is seeking candidates for a Sr. Industrial Engineer in the Wafer Industrial Engineering group located in Bloomington, MN.

Position Description: Responsibilities including: 1) Capacity -- detailing short & long term capacity requirements for an area of the Wafer Fab and working with Research & Development Engineering to outline future capacity needs according to their roadmap 2) Capital -- detailing capital equipment purchase requirements for an area of the Wafer Fab and organizing/developing capital justification packages to purchase new equipment sets 3) Lean Manufacturing -- supporting lean manufacturing activities for an area of the Wafer Fab including reducing non-value added activities, leading Overall Equipment Effectiveness (OEE) teams, and conducting multi-observation studies 4) Simulation Modeling -- developing and executing a plan for dynamic simulation modeling to predict bottlenecks, understand cycle time factors, and to recommend shop floor practice changes 5) Visual Basic Programming -- maintain a static capacity model (add functions and debug errors).

Experience: 4 to 7 years IE experience involving project management, simulation program development, and visual basic programming. Ability to conceive, plan, and execute complex projects under minimal direction with a high degree of professional competence. Require an advanced working knowledge of simulation program development, MS Excel, and Visual Basic. Prefer experiences in wafer fab manufacturing, lean manufacturing, capacity planning, AutoSched and AP simulation.

Education: Requires a Bachelor's degree in industrial engineering or related engineering field with 4-7 years IE type experience.

For more information, please contact Juan Manuel Torres, at Juan.M.Torres@seagate.com.

TPIC Conference Announcement

Roger Watson of jTask sent us this announcement: "I thought that FabTime's newsletter subscribers might be interested in the following links for the TPIC Annual Conference (Technician Performance Improvement Council, sponsored by SEMI and SEMATECH). This year's conference is entitled "Reduce Time to Performance." I'll be running a pre-conference workshop, **Measuring Training Mathematically**, there on Tuesday, July 30, where I'll be addressing problems such as:

- Verifying that what was promised in the course description was actually taught in class.
- Determining if a student believes he/she can actually perform a task to the required standard.
- Determining , through independent verification, if a student can perform a task at the end of a class.
- Evaluating instructor performance on real results - on the basis of whether or not students can actually perform a task at the end of a class.
- Determining , in real-time, the impact of overloading a class, mixing students of different skill levels in a class, or not having sufficient equipment.
- Showing management, quantitatively, the results of training in terms they understand.

There will be a lot of interesting ideas at the conference presented by companies such as Intel, AMD, KLA-Tencor, Sandia National Labs, and Agilent - to name a few - plus, of course, it's a great opportunity to mix with fellow SEMI professionals..."

TPIC Annual Conference: Reduce Time to Performance:

About: www.tpic.org/index.html
Schedule: www.tpic.org/TPIC-Agenda.html
Date: July 30 to Aug 1, 2002
Location: Albuquerque, New Mexico

Characteristic Curve Generator Update

Back in Issue 2.7 of the FabTime newsletter, we introduced an Excel-based characteristic curve generator. The characteristic curve generator was updated slightly in November of last year. We're now announcing another update. We have modified the characteristic curve generator to allow for coefficients of variation of greater than 1.0. This is because in a wafer fab the coefficient of variation of the time between arrivals to a toolgroup or operation is frequently quite a bit larger than 1.0 (where 1.0 is the coefficient of variation for exponential interarrivals). Therefore, we wanted to modify the characteristic curve generator to reflect this. In the process, we also fixed a small error that was introduced during the November update and affected the calculations in the third scenario. To download the updated characteristic curve generator, simply go to www.fabtime.com/charcurve.htm.

FabTime welcomes the opportunity to publish community news and announcements. Simply send them to Jennifer.-Robinson@FabTime.com.

Subscriber Discussion Forum

Wafer Starts Methodologies

Robert Hood of WaferTech wrote: "Are there any good papers on wafer starts methodologies? Any help would be appreciated."

FabTime Response:

A selection of the references that we have on lot release for wafer fabs are included below. We can't really vouch for which ones are "good", but these are all specific to semiconductor manufacturing and lot release.

We're in the process of adding some variability calculations to our FabTime software, so that the software can calculate the arrival process variability to each operation. This is a key component to cycle time. We looked at this for a simulation model that we have in which lots are released in batches of 10 at a time, and we observed high arrival process variability at the early operations in the fab, decreasing gradually throughput the process. We're planning to look at this for actual fab data, but that work is still in progress.

Our general feeling is that for good cycle time, you should release lots as smoothly as possible, though some research has suggested releasing in batches equal to the batch size of early furnace steps. Of course in practice fab management doesn't always have as much control over this as you might like.

If any other subscribers have observations on wafer start methodologies, or references that you have found particularly useful, we would love to hear about them. Just send them to Jennifer.Robinson@FabTime.com, and we will write about them in a future newsletter issue.

- N. Bahaji, "Simulation Study of the Effect of Dispatching Rules and Lot Release Strategies in Semiconductor Fabrication Facilities," Master's Thesis, Louisiana State University and Agricultural and Mechanical College, Department of Industrial and Manufacturing Systems Engineering, December 2000.

- Y. D. Kim, D. H. Lee, J. U. Kim, and H. K. Roh, "A Simulation Study On Lot Release Control, Mask Scheduling, And Batch Scheduling In Semiconductor Wafer Fabrication Facilities," Journal of Manufacturing Systems, Vol. 17, No. 2, 107-117, 1998.

- J. Kim, R. C. Leachman, and B. Suh, "Dynamic Release Control Policy for the Semiconductor Wafer Fabrication Lines," Journal of the Operations Research Society, Vol. 47, No. 12, 1516-1525, 1996.

- R. McKiddie, "Some No-Panic Help for Wafer-Start Surges, Semiconductor International, 115-120, June 1995.

- R. Sandell, "Scheduling Policies in Semiconductor Manufacturing Systems SEMATECH Technology Transfer # 95062884A-XFR, July 31, 1995. (Email Jennifer.Robinson@FabTime.com for a PDF copy of this paper.)

Operator Modeling

Another subscriber wrote: "As we consider increasing staffing at our plant due to increased demand for our product, I have been mulling over specific ways to justify operator headcount increases. There are several ways you **could** quantify the optimal number of operators (based on inventory or # tools) but I was wondering if you know of any research or papers out there that address this issue... Just curious what the experts in the industry say about this issue. So far, the decision for deter-

mining optimal headcount seems to be more of a guess, rather than any type of mathematical model..."

FabTime Response:

The Factory Explorer capacity and simulation analysis tool can generate headcounts. You specify, for each toolgroup in the model, what percentage of time the operator is required for loading, processing, and unloading wafers. At each process step, you specify the operator group required for processing, and optionally for transport. Then FX calculates the required number of operators in each group, based on the product mix. You can enter operator break schedules, and specify how heavily you would want each operator group loaded. This is a very detailed approach, because it relies on having a simulation / capacity model that specifies the process times at each step. And you still have to make an assumption about how heavily you want the operator groups to be loaded. (For more information see www.wwk.com - Frank Chance was the developer of FX, but it is now owned by Wright Williams & Kelly).

One study that used FX to explore operator planning is R. C. Kotcher, "How "Overstaffing" at Bottleneck Machines Can Unleash Extra Capacity," Proceedings of the 2001 Winter Simulation Conference, Washington, D.C., 1163-1169, 2001. This paper can be downloaded at no charge from the INFORMS College of Simulation website, at www.informs-cs.org/wsc01papers/prog01.htm#SE.

Some other references that we have on operator planning for wafer fabs include:

- W. Chou and J. Everton, "Capacity Planning For Development Wafer Fab Expansion," Proceedings of the 1996 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, Cambridge, MA, 17-22, 1996.

- D. S. O'Ferrell, "Manufacturing Modeling and Optimization," Proceedings of the 1995 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, Cambridge, MA, 334-339, 1995.

- S. A. Mosley, T. Teyner, and R. M. Uzsoy, "Maintenance Scheduling And Staffing Policies In A Wafer Fabrication Facility," IEEE Transactions on Semiconductor Manufacturing, Vol. 11, No. 2, 316-323, 1998.

- A. Raviv, "Applications of Queuing Theory and Simulation to Staffing in the Semiconductor Clean Room Environment," Proceedings of the 1995 IEEE/UCS/SEMI International Symposium on Semiconductor Manufacturing, Austin, TX, 252-256, 1995.

Other commercial labor planning tools are also available. Abbie Gregg, Inc. (FabTime's sales and implementation partner for Arizona and New Mexico) has a labor model called Io. Io is an add-on to AGI's Jupiter Factory Product/Cost Model. Io uses queueing approximations to explore cost/labor/capacity trade-offs. More information is available at AGI's website, www.abbiegregg.com (under Products). Tefen (www.tefen.com) also has a labor planning model, although FabTime is less familiar with this product. Their Staffware product is a queueing based staffing model designed for the semiconductor industry.

Ramp Literature/Models

Another subscriber asked: "Do you have literature/models for ramping up the production in the semiconductor industry?"

FabTime Response:

There is a SEMATECH paper on the subject that was written several years ago (the first reference below). I have the

document in PDF, if anyone is interested. I've also included several other references that deal with wafer fab ramping in various ways (but not including yield ramp). It seems to me that there should be more work in this area (the industry is constantly ramping up or down). If any other subscribers have anything to add on this topic, please let us know. Hopefully there will be lots of ramping up soon!

- N. Abt, S. Dick, T. Jefferson, and L. Solomon, "Ramp Up Analysis for Semiconductor Manufacturers," SEMATECH Technology Transfer #94122642A-XFR, 1995.

- F. G. Boebel, "Quintuple Ramp Up Slope By Implementing Cross-Functional, Self-Directed Work Teams," Proceedings of the 1996 Advanced Semiconductor Manufacturing Conference, 436-441, 1996.

- J. Fritz, J. Benjamin, and R. Rerick, R. "Wafer Fab Conversion Through Theory of Constraint Project Management Techniques," 10TH Annual IEEE/SEMI Advanced Semiconductor Manufacturing Conference and Workshop, 202-203, 1999.

- J. Lubash and A. Porter, "Greenfield Planning Using Innovative Analytical Tools," Proceedings of the 1997 IEEE/SEMI Advanced Semiconductor Manufacturing Conference, 162-165, 1997.

- M. Montier and M. Henry, "Advanced R&D to Volume Production in 300 mm," Proceedings of the 1999 International Interconnect Technology Conference, 9-11, 1999.

Treating Scrap in Product Costing

Another subscriber asked "I wonder if you know how most companies treat yield losses? Do they include the cost of yield losses in the cost of the product? Charging a customer for what is essentially a "waste" isn't a sound practice. But then, how would a company account for the cost of scrap?"

FabTime Response:

The thing that makes product costing difficult in semiconductor manufacturing is that most of the costs are fixed costs (fab and equipment) rather than variable costs that can be directly attributed to products. So costing often ends up being done on some sort of allocation basis. In terms of scrap, what we've seen is that companies derive product costs by taking their total costs and then allocating them by some methodology to the good units out. That's one way to do product costing, and in that case, customers are implicitly charged for the scrapped wafers. I would imagine that in other cases, product prices are determined according to what the market will bear. Certainly if you have less scrap, you could afford to charge less for your good products. On the other hand, if you provide bleeding edge new technology products, you will likely have more scrap, but will be able to charge a higher price.

If any readers have anything to contribute in response to this question, please write to Jennifer.Robinson@FabTime.com.

Calculating Mean Time Between Assists

Another newsletter subscriber asked about calculating the mean time between assists (MTBA) for die bonders. "To bond a die exactly on the right place on a substrate you have to tell the machine the position. Therefore the substrate has fiducials on it for which the machine's cameras search. Then the machine calculates the distance between fiducial and bonding position and so on. If the camera couldn't find the fiducials, the operator gets a message "fiducial not found" on the operator screen. This message has to be acknowledged, then the machine starts fiducial search again. To confirm the message

"Fiducial not found" takes approximately 8-12 sec. Most of the errors occur not because the machine can't find the fiducials, but because the quality of the substrates are poor. My question is whether or not it is acceptable to leave these "fiducial not found" errors out of the MTNA calculations."

FabTime Response:
This is outside of our area of expertise, and so we defer to other newsletter subscribers to address this issue.

The Bottom-Line Benefits of Cycle Time Management

Introduction

Over the past three years, we've had a number of discussions with people throughout our industry on the topic of cycle time management and its financial return. In general, we've found that people believe shorter cycle times are a Good Thing. However, the link between shorter cycle times and improved financials remains murky. In this discussion, we'll present our thoughts on how this murkiness can be quantified. The end-result is an Excel spreadsheet that estimates the dollar-impact of shorter cycle times.

Consumer Protection Warning

We'll be using averages and estimates for the inputs in our model. This is just a starting point. Every fab is unique, so the spreadsheet won't apply to your fab unless you modify the inputs. Also, you will need to consider the assumptions underlying each potential benefit. For example, if the benefit is increased production of a product you can't currently sell, then you won't be improving your profits one bit!

From Cycle Time to Dollars

The first step in our quantification process is to lay out the paths by which an improvement in cycle time may be reflected on the bottom line. To be useful, these paths must ultimately lead to increased revenues or decreased expenses, so we'll group paths into these two high-level categories. If you'll recall, back in issue 2.6 of this newsletter we discussed several of these paths, with the focus on one in particular - reduced inventory write-offs during a downturn. This month, we'll include that path plus a number of others in one consolidated spreadsheet.

Expense-Related Paths

E1) Raw Materials Savings - Yield Improvements:
Shorter production cycle times → Improved yield → Fewer starts required for same throughput → Decreased raw material costs → Decreased expense.

E2) ECN (Engineering Change Notice) Savings - Decreased WIP:
Shorter production cycle times → Decreased production WIP → Fewer lots requiring ECN rework → Decreased expenses.

E3) Finished Goods Write-Off Savings - Decreased Safety Stock Required:
Shorter production cycle times → Decreased safety stock required for finished goods inventory → Decreased risk of inventory obsolescence → Decreased write-offs of inventory → Decreased expense.

E4) WIP Carrying Cost Savings:
Shorter production cycle times → Decreased WIP → Decreased WIP investment

→ Decreased WIP carrying costs → Decreased expense.

Revenue-Related Paths

R1) Design Wins - Increased Cycles of Learning:
Shorter R&D cycle times → More cycles of learning during product development → More time for experimentation and product refinement → More competitive products → Increased design wins → Increased revenue.

R2) Design Wins - First to Market:
Shorter R&D cycle times → Faster product development → First to market → Increased design wins → Increased revenue.

R3) Pricing Premium - First to Market:
Shorter R&D cycle times → More cycles of learning during product development → Faster product development → First to market → New product pricing premium → Increased revenue.

Quantification and Inputs

We have quantified these paths in a spreadsheet that can be found on our website at www.FabTime.com/bottomline.htm. (Note that this spreadsheet replaces the earlier cycle time benefits calculator that was available from FabTime's website.) The first worksheet, Calculator, contains a summary of inputs and benefits. The second worksheet, Details, contains the detailed calculation behind each benefit. The third worksheet, Notes, contains notes and references.

Several of the benefit calculations use inputs for which you may not know an exact value. For example, benefit R1 (Design Wins due to Increased Cycles of Learning) has these inputs:

(Current R&D Cycle Time)
(Target R&D Cycle Time Improvement)
(Weekly Wafer Outs)
(Workweeks per Year)
(Good Devices per Wafer Out)
(Revenue per Device)
(Current Design Wins per Year)
(New Product Pct) = "Percent of shipments that are new products (design wins from prior 12 months)"
(Design Win Factor1) = "Percent increase in design wins per additional R&D learning cycle"

And these calculations:

R1.1) (New Product Volume) = (Weekly Wafer Outs) * (New Product Pct) / (Current Design Wins per Year) * (Workweeks per Year)

R1.2) (Current Learning Cycles) = 365 / (Current R&D Cycle Time)

R1.3) (Improved Learning Cycles) = 365 / (Improved R&D Cycle Time)

R1.4) (Additional Learning Cycles) = (Improved Learning Cycles)-(Baseline Learning Cycles)

R1.5) (Additional Design Wins) = (Additional Learning Cycles) * (Design Win Factor1) * (Current Design Wins per Year)

R1.6) (Additional Wafers) = (Additional Design Wins) * (New Product Volume)

R1.7) (Additional Devices) = (Additional Wafers) * (Good Devices per Wafer Out)

R1.8) (Additional Revenue) = (Additional Devices) * (Revenue per Device)

The only input that is likely not estimable from existing fab data is

(Design Win Factor1) = "Percent increase in design wins per additional R&D learning cycle"

But it should be possible to provide a reasonable range of values. One additional R&D learning cycle per year could increase design wins by 1% to 5%, but it probably won't increase design wins by 25%.

Example

The spreadsheet on our website contains sample inputs for a fab with these characteristics:

- 500 wafer outs per week
- 50 day production cycle time
- 25 day R&D cycle time
- 90% line yield

The cycle time management targets are:

5% improvement in production cycle time
5% improvement in R&D cycle time

For the remaining inputs, we have entered values based on past experience, or for factors such as (Design Win Factor1), estimates that strike us as reasonable and conservative.

The resulting bottom-line benefits are:

$76,313	E1: Raw Material Savings
$24,802	E2: ECN Savings
$34,105	E3: F.G. Write-Off Savings
$62,500	E4: WIP Carrying Cost Savings
$100,855	R1: Design Wins - Learning
$164,063	R2: Design Wins - Time to Mkt
$82,031	R3: Pricing Prem. - 1st to Mkt
$544,668	Total Annual Benefit of CTM

Notice how the revenue-based benefits are larger than the expense-based benefits. This is a pattern we have seen in the past. In general, it matches our intuition that improvements in cycle time are quite valuable on the customer side of the equation (revenue). If you experiment with the spreadsheet, you will find that improvements in R&D cycle time generally have a bigger impact than improvements in production cycle time. This behavior is due to benefit paths R1, R2, and R3, which are all premised on an improvement in R&D cycle time. It is certainly possible that other benefit paths exist for improvements in production cycle time. Again, however, this behavior matches our intuition - cycle time is quite valuable when you are pushing to bring a new product to market, to get it into customers' hands for the very first time.

Even without the revenue-based benefits, however, the expense savings are significant.

Saving Time with Software

In our next issue, we'll return to the nuts and bolts of cycle time management, including three selected cycle time management styles. As part of that discussion, we'll cover the infrastructure (reports, alerts, analysis) that supports cycle time management. Providing this infrastructure - cycle time management software - is what keeps FabTime in business (and makes this newsletter possible!).

One benefit we have seen with our customers stems from the software itself, rather than from cycle time improvement. This benefit is the time-savings gained from automating the cycle time management infrastructure with FabTime. Shift supervisors, module managers, and production control personnel can spend a significant amount of time each day pulling data from disparate sources and massaging this data into useful information. Measured across the fab, the time-savings can easily add up to the equivalent of one full time manager.

While these savings do not flow directly from reduced cycle times, and thus are not included in the spreadsheet, we believe they are worth mentioning. As Peter

Drucker points out, a manager's time is the only 100% inelastic raw material upon which a company relies. No amount of money will ever supply more than 168 hours a week. Our goal is to minimize the data collection drudgery, thus freeing managers' time for more useful activities - such as managing!

Summary

Quantifying the benefits of cycle time management is a useful exercise. It puts the focus on areas where the potential return is greatest, thus clarifying our priorities. It also serves as a benchmark for post-improvement analysis: if the cycle time improvement targets have been achieved, were the predicted benefits obtained?

Acknowledgements

We would like to thank Ken Beller, of the FabTime advisory board, for his contributions during the brainstorming phase of this project, particularly in the identification of the various benefit paths. Thanks are also due to a newsletter subscriber who pointed out the double-counting of yield benefits in an earlier version of this spreadsheet - if there is an improvement in yield, you can either sell the additional wafers (thereby realizing a increase in revenue), or start fewer wafers (thereby realizing a decrease in raw wafer expenses), but not both. In the current model we resolve this issue by accounting for yield benefits entirely as a reduction in raw wafer expenses.

Further Reading

For more about the inelasticity of a manager's time, we recommend "The Effective Executive" by Peter Drucker. You can find a review, and a link to purchase the book from Amazon, at http://www.fabtime.com/effective.htm.

For a discussion on the cost of delays in new product introductions, see D. Kinkead, J. Mastrobuono, K. Dean and W. Trybula's "The Cost of Imperfect Wafer Environmental Control," Semiconductor International, June 2001, p. 135. This paper suggests that each day of delay in ramping a new DRAM product to volume production costs $2.5M over the lifetime of the product. This paper is available through the archives on the Semiconductor International website. Since it is more than 6 months old, you will need to register.

FabTime Recommendations

FabTime Book Review - Next: The Future Just Happened

In this book, Michael Lewis explores how the Internet has encouraged changes in the way people live their lives. While he doesn't view the Internet as causing revolutionary change, he does see it as a tool that facilitates certain trends already in progress. These trends include the flattening of hierarchies, the development of closer relationships between insiders and outsides, and the increased influence of younger and younger individuals in technological areas.

Lewis spends considerable time describing three particular teenagers who represent different instances of trends exaggerated by the availability of Internet access. For all three teenagers, the Internet allowed

them to use masks to reinvent themselves, and challenge figures of central authority. The book is a little bit fragmented. The two last sections are about how the Internet is changing the traditional models of television advertising and polling, and about the backlash against technology by certain technology pioneers, while interesting, are very distinct from the first two sections. Overall, however, the use of stories about and interviews with real people make this book a fun and interesting read. Lewis has a knack for making the reader think about the larger issues, without laying down the law about what the reader "should" be thinking. A link to order this book is available at www.FabTime.com/next.htm.

Blackmask E-Books

Blackmask bills itself as "a provider of Internet literature." The site is maintained by David Moynihan, a former English major who seems to really love books. David maintains a large selection of both mostly free e-books - currently at 7,909 selections, with new ones added every business day. Most of the books are provided in various formats for different readers: html, Ms-Reader, Acrobat, Rocket eBook, zipped, etc. This is probably not the most comprehensive directory of electronic texts that you could find out there, but it is well-organized, and has some interesting selections. You can also buy David's own books for a small fee - self-publishing in the Internet age. This website is at www.blackmask.com.

Subscriber List

Total Subscribers: 872
1st Silicon (3)
3M Company (5)
Abbie Gregg Inc. (6)
ABB (5)
ADC (1)
Adexa Corporation (1)
Advanced Micro Devices (40)
Advanced Sound Products (1)
Affymetrix (1)
Agere Systems (5)
Agilent Technologies (7)
Aisin Indonesia (1)
Alfalight Canada (1)
Alpha Industries (2)
Alpha-Sang (1)
AMI Semiconductor (2)
Amkor (4)
AMR Research (1)
Analog Devices (5)
Andes University (1)
Applied Materials Corporation (11)
Aralight Corporation (2)
Arch Wireless (1)
Arizona State University (6)
Arkansas Tech University (1)
Asia Management Group (1)
ASM International NV (1)
ASML (4)
ATMEL (5)
Australian National University (1)
Automatiseringsteknik (1)
Axcelis Technologies (1)
Axsun Technologies (1)
Babson College (1)
Bookham Technology Plc (1)
Boston Scientific (1)
Bovis Lend Lease Microelectronics (1)
BP Solar (3)
Brooks Automation (3)
Byelorussian State Economic Univ. (1)
Cabot Microelectronics Ltd. (1)
California Micro Devices (2)
California Polytechnic State University (2)

C&D Aerospace (1)
Cannon Precision (1)
Canon USA (1)
Carsem M Sdn Bhd (3)
Chartered Semiconductor Mfg (26)
CMC Electronics (1)
CNRI (1)
Communicant (1)
Compugraphics International Ltd. (1)
Conexant Systems, Inc. (4)
Continental Device India Ltd. (1)
Cornell University (1)
Corning (1)
Cox High Speed Internet (1)
C-Port Corporation (1)
Cree, Inc. (1)
Cronos Integrated Microsystems (1)
Cummins S. de R.L. de C.V. (1)
Cyberfab (1)
Cypress Semiconductor (1)
CyTerra Corporation (1)
Dallas Semiconductor (3)
DALSA Semiconductor (2)
Datacon Semiconductor Equipment (1)
Delphi Automotive Systems (2)
Delta Design (1)
Dick Williams and Associates (1)
Digital Optics Corporation (2)
DomainLogix Corporation (1)
Dominion Semiconductor (5)
Dow Corning Corporation (1)
Durham ATS Group (4)
Dwarkadas Associates (1)
Eastman Kodak Company (3)
Electroglas, Inc. - Statware Division (2)
e-METS Co, Ltd (1)
Ernst & Young (1)
eSilicon Corporation (1)
Eskay Corporation (1)
FabOptima GmbH (1)
FabTime (3)
Fairchild Imaging (1)
Fairchild Semiconductor (3)
Fort Wayne Wire Die (1)
Fraunhofer IPA (1)
Front Line Performance (1)
Fujitsu Microelectronics, Inc. (1)
Gebze Institute of Technology (1)
Genmark Automation (1)
Georgia Tech (1)
Gintic Institute of Mfg. Technology (1)
Headway Technologies (4)
Hewlett-Packard Company (6)
Hitachi, Ltd. (1)
Hitachi Nippon Steel Semiconductor (4)
Huck Fasteners (1)
Hynix Semiconductor Mfg America Inc. (1)
i2 Technologies (1)
IBM (11)
ICF Consulting (1)
ICG / Semiconductor FabTech (2)
IDC (7)
IMEC (2)
Infineon Technologies (35)
Infosim Networking Solutions (1)
INNOTECH Corporation (2)
INSEAD (3)
Institut National Polytech. de Grenoble (2)
Integrated Device Technologies (2)
Integrated Technologies Company (2)
Intel Corporation (38)
Intelligent Quality Systems (1)
International Rectifier / HEXAM (6)
Intersil (3)
Interstar Technology (1)
ITI Limited (1)
IZET Innovationszentrum Itzehoe (1)
Jacobs Consultancy (1)
James Nagel Associates (1)
JDS Uniphase (3)
Kansas State University (1)
Ken Rich Associates (1)
KLA-Tencor (1)
Kulicke & Soffa Industries, Inc. - K&S (1)
Kymata - Alcatel (1)
Lexmark International, Inc. (1)
Linear Technology (1)
Litel Instruments (2)
LSI Logic (10)
M2M Group (1)
Lynx Photonic Networks (1)
Macronix International Co. (5)
Managed Outsourcing, Inc. (2)
MASA Group (1)
Maxim Integrated Products, Inc. (3)
MMC Technology (1)

Medtronic (6)
MEMS Optical (1)
Methode Electronics, Inc, (1)
Metrology Perspectives Group (1)
Micrel Semiconductor (2)
Microchip Technology (1)
Micron Technology, Inc. (1)
MicroVision-Engineering GmbH (1)
Mitsubishi Semiconductor Europe (2)
Motorola Corporation (47)
MTE Associates (1)
Nanometrics (1)
Nanyang Technological University (4)
National Chiao Tung University (1)
National Semiconductor (12)
National Univ. of Ireland - Galway (1)
National University of Singapore (2)
NEC Electronics (8)
Nortel Networks (7)
Ohio State University (1)
Oklahoma State University (1)
ON Semiconductor (8)
Onix Microsystems (1)
OPTUM-IES (1)
Palmborg Associates, Inc. (2)
Pelita Harapan University (1)
Penn State University (3)
Peter Wolters CMP Systeme (1)
Philips (20)
Piezo Technology Inc. (1)
Planar Systems (2)
PolarFab (3)
Politecnico of Milano (1)
Powerex, Inc. (3)
PRI Automation (2)
Productivity Partners Ltd (1)
ProMOS Tech. (1)
Propsys Brightriver (1)
PSI Technologies, Inc. (1)
Quanta Display Inc. (1)
Ramsey Associates (1)
Raytheon (2)
Read-Rite Corporation (4)
Redicon Metal (1)
Rexam (1)
Rockwell Automation (1)
RTRON Corporation (2)
SAMES (1)
Samsung (14)
Samtel Electron Devices GmbH (1)
Saint-Gobain Company (1)
SAP AG (1)
Seagate Technology (19)
SEMATECH (18)
Semiconductor Research Corp. (1)
SemiTorr NorthWest, Inc. (1)
Senzpak Pte Ltd. (1)
Serus Corporation (1)
SEZ America, Inc. (1)
Shanghai Grace Semiconductor Mfg. (1)
SiGen Corporation (1)
Silicon Integrated Systems Corp (1)
Silicon Manufacturing Partners (4)
Silterra Malaysia Sdn. Bhd. (4)
Sipex Corporation (1)
Sony Semiconductor (2)
SoundView Technology (4)
Southern Wire Industries (1)
SSMC (2)
STMicroelectronics (33)
Stonelake Ltd. (1)
Storage Technology de Puerto Rico (1)
Superconductor Technologies, Inc. (1)
Süss MicroTec AG (2)
Synquest (2)
Takvorian Consulting (1)
TDK (1)
Technische Universitat Ilmenau (1)
TECH Semiconductor Singapore (20)
Terosil, a.s. (1)
Texas A&M University (1)
Texas Instruments (13)
Tokyo Electron Deutschland (1)
Tower Semiconductor Ltd. (1)
Toyota CRDL (1)
Triniti Corporation (1)
TriQuint Semiconductor (8)
Tru-Si Technologies (1)
TRW (1)
TSMC (4)
UMC (7)
Unisem (1)
United Monolithic Semiconductors (2)
Unitopia Taiwan Corporation (2)
Universidade Federal de Santa Catarina (1)
University of Arkansas (1)

University of California - Berkeley (5)
University of Cincinnati (1)
University of Missouri-Columbia (1)
University Porto (1)
University of Texas at Austin (1)
University of Virginia (1)
University of Wuerzburg - Germany (1)
Velocium (1)
Virginia Tech (9)
Vishay (1)
Vitesse Semiconductor (1)
Voltas Limited (1)
Wacker Siltronic (3)
WaferTech (11)
Win Semiconductor (1)
Wright Williams & Kelly (8)
Xerox Brazil (1)
X-FAB Texas, Inc. (3)
Yonsei University (1)
Zarlink Semiconductor (2)
Zetek PLC (1)
ZMC International Pte Ltd (2)
Unlisted Companies (14)

Consultants:
Carrie Beam
Vinay Binjrajka (PWC)
Javier Bonal
Steven Brown
Stuart Carr
Alison Cohen
Paul Czarnocki
Scott Erjavic
Greg Fernandez
Ted Forsman
Navi Grewal
Cory Hanosh
Norbie Lavigne
Michael Ray
Bill Parr
Nagaraja Jagannadha Rao
Lyle Rusanowski
Mark Spearman (Factory Physics, Inc.)
Dan Theodore
Craig Volonoski

Note: Inclusion in the subscriber profile for this newsletter indicates an interest, on the part of individual subscribers, in cycle time management. It does not imply any endorsement of FabTime or its products by any individual or his or her company. To protect the privacy of our subscribers, email addresses are not printed in the newsletter. If you wish contact the subscribers from a particular company directly, simply email your request to the editor at Jennifer.Robinson@FabTime.com. To subscribe to the newsletter, send email to the same address. You can also subscribe online at www.FabTime.com/newsletter.htm. We will not, under any circumstances, give your personal information to anyone outside of FabTime.