# FabTime Cycle Time Management Newsletter

Volume 2, No. 8 October 2001

## Information

**Mission:** To discuss issues relating to proactive wafer fab cycle time management.

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## Welcome

Welcome to Volume 2, Number 8 of the FabTime cycle time management newsletter. The world has changed since our last issue went out in late August, and we at FabTime would like to extend our sympathy to anyone who suffered losses from the events of September 11th. In addition to the overwhelming personal aspects to the tragedy, this situation has almost surely pushed out the recovery in the semiconductor industry by another few months. But Americans are resilient, and the semiconductor industry is resilient, and I think that we will get back on track.

In this issue, we have two press releases of which we're especially proud. First, we recently donated a license for FabTime to the University of Arkansas, to be used in Scott Mason's Razorback Electronics Manufacturing lab. Second, we have completed the installation of our FabTime cycle time management software system at AMD's Fab 25 in Austin. We would especially like to thank Mike Hillis of AMD for being a great project manager during the installation.

We also have some great feedback from readers, in response to the last newsletter issue. Peter Gaboury of ST shared a number of his observation on process time variability, while others send in requests for clarification and additional detail. In this new issue we're going to discuss goal setting in a wafer fab, with an article written by Frank Chance.

Thanks for reading! -- Jennifer

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# Community News/Announcements

## FabTime Donates Cycle Time Management Software to University of Arkansas

Menlo Park, CA. September 26, 2001 - FabTime Inc. today announced that it had donated a license for its FabTime cycle time management software to the University of Arkansas. The software will be used by the Razorback Electronics Manufacturing (REM) Lab within the Department of Industrial Engineering.

Professor Scott Mason, director of the REM Lab said, "We intend to use FabTime to support our research in wafer fab scheduling. The software will give us a flexible window into fab performance under different scheduling policies, and help us to measure the impact of these scheduling policies on cycle time and equipment utilization."

"We are excited to be working with the University of Arkansas," said Jennifer Robinson, Chief Operating Officer of FabTime. "Although FabTime was designed for real-time analysis of existing wafer fabs, the REM Lab will be able to use it as a graphical tool for in-depth analysis of simulated fab operations. I think that Professor Mason and his students will provide feedback that will help us to make the software even more useful for this type of analysis in the future."

Corporate customers for FabTime's cycle time management software include Advanced Micro Devices (NYSE: AMD) and Headway Technologies, a division of TDK (NYSE: TDK). A form for requesting more information about the software, including university licensing options, is available at www.fabtime.com/software.htm.

About the Razorback Electronics Manufacturing Lab:

The Razorback Electronics Manufacturing Laboratory (REM Lab) is a research facility located in the Engineering Research Center of the University of Arkansas. The lab is dedicated to advancing the current state of the art in semiconductor manufacturing scheduling research and to preparing trained engineers to enter this challenging field. The primary focus of research is on improving manufacturing schedules to increase utilization of equipment. The website for the lab is at www.uark.edu/~remlab/.

## FabTime Completes Cycle Time Management System Installation at AMD's Fab 25

Menlo Park, CA. October 5, 2001 - FabTime Inc. today announced that it had completed the installation of its FabTime cycle time management system at AMD's Fab 25 in Austin, TX. Fab 25 has more than 100,000 square feet of cleanroom space, and was designed to support several generations of process technology. AMD selected FabTime's software to aid in cycle time improvement efforts at Fab 25.

"I've been using FabTime's lot-tracking features to accelerate hot lots and to get immediate notification of scrap-related problems," said Mike Hillis, Fab 25 Cycle Time and Line Yield Improvement Manager. "FabTime enables shift facilitators to monitor performance in their areas better, in order to improve cycle time and activities. Instead of spending time preparing reports, they can get the data they need quickly from FabTime, and then spend their time making real improvements."

"The Fab 25 installation project has been a great success for FabTime," said Frank

Chance, President of FabTime. "We've made numerous enhancements to the software based on AMD's feedback. It will definitely be a more useful product for other customers thanks to AMD. Now that the installation is complete, we look forward to supporting AMD on specific cycle time improvement projects."

FabTime is designed to give wafer fab managers and their staff the information that they need, in real-time, to run their fabs effectively. FabTime extracts lot move transaction data from the fab manufacturing execution system (MES) every five minutes, and imports this data into a SQL Server database. Users can then access a comprehensive system of cycle time-related charts and alerts via a web browser from anywhere within the corporate Intranet. More information can be requested from www.FabTime.com/software.htm.

### About AMD

AMD is a global supplier of integrated circuits for the personal and networked computer and communications markets with manufacturing facilities in the United States, Europe, Japan, and Asia. AMD, a Fortune 500 and Standard & Poor's 500 company, produces microprocessors, flash memory devices, and support circuitry for communications and networking applications. Founded in 1969 and based in Sunnyvale, California, AMD had revenues of $4.6 billion in 2000. (NYSE: AMD).

## International Symposium on Semiconductor Manufacturing (ISSM) Proceeds as Planned

AUSTIN, Texas (25 September 2001) - The International Symposium on Semiconductor Manufacturing (ISSM), a premier industry forum for semiconductor manufacturing professionals to explore trends in manufacturing science and technology, will take place October 7-10, 2001 as planned. The annual symposium, now in its 10th year, will also feature presentations by industry leaders that address strategies to confront the current industry recession and visions for revitalizing the semiconductor industry.

"ISSM and the industry that it represents unite technologists in an effort to advance society, to bring the world closer together, and to help build a brighter future," said Bruce Sohn, program and technical chair of the symposium. "We also hope to find ways to deal with, if not overcome, the current recession."

ISSM 2001 will feature speakers from 83 different semiconductor organizations from 14 nations. All oral presentations will be simultaneously interpreted between English and Japanese. In addition to the keynote speakers, more than 125 poster presentations will be offered.

Two special workshops are also being held in conjunction with ISSM. The first workshop focuses on the current transition to 300mm wafers and features speakers from Intel, International SEMATECH, Selete, Trecenti, TSMC, and Wacker. The second workshop explores future needs of semiconductor manufacturing beyond the 70nm technology node. Laying out key strategies are senior technologists from Clemson University, Intel, International SEMATECH, KLA-Tencor, Selete, the Semiconductor Research Corporation (SRC) and Texas Instruments.

The symposium will be held at the Fairmont Hotel in San Jose, California. Details, including speakers, complete program and conference registration are available at the ISSM web site (www.issm.com) or by contacting Audrey Measel at Meetings Plus at 925-287-5388.

# Responses to Previous Newsletter Topics

## Operating (Characteristic) Curve for Test

A reader from Germany wrote: "Your newsletter is very interesting for me. Now I have a question. I created a operating curve for our wafer test area. It seems that it works really good. We realize the overall effects as shown in the curve for the wafer test and it corresponds with our impressions of the situation in the past. Now I would like to get information/experiences from you or other readers who worked with operating curves in the wafer test area. (For instance about typical effects like variable test time)"

### FabTime response:

We were involved in a simulation study with Infineon Technologies several years ago in which several cycle time reduction opportunities for back-end facilities (including test) were investigated. The paper can be requested from our website, by filling out the paper request form at www.FabTime.com/request.htm, and selecting the following paper:

J. Domaschke, S. Brown, J. K. Robinson, and F. Leibl, "Effective Implementation Of Cycle Time Reduction Strategies For Semiconductor Back-End Manufacturing."

In this study, the test area was the system constraint. Potential improvements were explored using characteristic curves (also called operating curves). Operating changes for test included a test procedure change (which reduced the load on the bottleneck), a modification to test handler dedication strategies, and a change in staffing policies. These changes, along with other back-end changes, indicated that cycle time could be reduced cumulatively by 41% for the back end facility. After several of the recommendations were implemented, actual cycle times decreased by about 32% (under changes in product mix and volumes).

A related paper (describing the same study) is also available from our website, under:

S. Brown, J. Domaschke, and F. Leibl, "Cycle Time Reductions for Test Area Bottleneck Equipment."

I also looked through a bibliography that I maintain, and found a couple of other references that might be relevant to this question:

- J. D. Liljegren, "Modeling Final Assembly and Test Processes in the Semiconductor Industry," *Proceedings of the 1992 Winter Simulation Conference*, (eds.) J. J. Swain, D. Goldsman, R. C. Crain, and J. R. Wilson, 856-860, 1992.

- D. D. Sheu, J. Lin, and P. Liao, "Benchmarking Manufacturing Management Of Taiwan's IC Packaging Plants," *International Journal of Industrial Engineering*, Vol. 7, No. 4, 365-370, 2001.

- A. W. Chan, A. Satir, and V. J. Thomson, "Reduction of Cycle Time in Manufacturing Using Simulation," *Proceedings of the International Conference on Computer Applications in Production and Engineering (CAPE '97)*, Detroit, MI, 359-368, November 1997.

- P. Chandra and S. Gupta, "Managing Batch Processors to Reduce Lead Time in a Semiconductor Packaging Line," *International Journal of Production Research*, Vol. 35, No. 3, 611-633, 1997.

I don't know of any other studies that involved working with operating curves for test, and so I put this question to our other readers. If anyone has anything to contrib-

ute on this subject, please write to Jennifer.Robinson@FabTime.com, and I will pass the information along during the next issue.

## Feedback on Process Time Variability

Peter Gaboury (STMicroelectronics) wrote: "An interesting article on variability. I am sure that in the next few years the companies that focus on variability will be able to break the utilisation-cycle time compromise.

Just a couple of comments:

⇒ Take a look at the most recent issue of Future Fab (Issue 11) - I published a paper on measuring process time variability (and discussed some solutions on how to decrease it ...). In the paper I analysed the process time variability on 5 different types of machines and using the ANOVA technique - broke down the variability into its fundamental components (Job to Job, Wafer-Wafer, Lot-Lot, Within Wafer (example variability between process times of wafer 1),... I collected data automatically by using the automation system - permitting me to analyse a very large sample. I found some interesting things:

- Don't assume that process time variability is negligible. I found coefficients of variation from 1.39 (good) to 3.38.

- The etcher had the lowest process variability - whereas there is certainly a trade off in maintenance variability - i.e. the etcher probably has the highest maintenance variability.

- The contributors to variability are not always the same. For example on one machine the variability of the process times for wafer 1 was the most significant (i.e. wafer 1 to wafer 1 process time variation) whereas on another machine the impact of the process time of wafer 1 versus the other wafers was the most significant (i.e. wafer 1 compared to wafer 2 to 25).

The key message of my paper is that people need to start measuring process time so that they can focus on the correct components of variability.

⇒ I think fundamentally people need to start measuring "Maintenance" Variability - not typically done in fabs. Take a look at the distribution of variability of different machines in the fab and try to understand which machine has the most variability. I hope for their sake that this machine is not a bottleneck.

⇒ We need to think about "line engineering" and choosing the GOOD bottleneck based on variability. Having an etcher as a bottleneck is not a good choice - unless you are very stable in your cleaning maintenance. Having a nitride dep - is suicide.

Fortunately - the photo tools are from a maintenance standpoint very stable (an additional argument from the most expensive) - however from a process time standpoint - a lot of work needs to be done (reject wafers, alignment mark capture, assists, rework, ...).

⇒ Lastly - I think that we need to find SIMPLE metrics to measure variability - so that we can drive improvement quickly. One company that I know measures the differences in the availability distribution and looks at where is 20% of the data and where is 80% of the data - looking at the spread between 20 and 80.

For process time variability and arrival time variability - honestly I am at a loss to find a simple metric that you can track to look at improvement. Your feedback?"

**FabTime response:**
Thanks for taking the time to write such a thoughtful and detailed response to the article on variability. I have looked at your Future Fab paper (www.future-fab.com/documents.asp?grID=212&d_ID=637, and think that it gives a great discussion of the issues related to process time variability in wafer fabs (Readers: I definitely recommend that you check out the paper - you can download it in PDF format from the Future Fab website).

I agree with you that measuring process time variability and maintenance variability could be very helpful for cycle time improvement efforts. For example, you could identify whether high cycle times through a particular tool were due to process time variability or repair time variability, to help focus improvement efforts. You could also sort by coefficient of variability, to see which tools (or operations) stand out as problems. These could be causing cycle time problems downstream, even where the high process and maintenance variability tools themselves might not have high cycle times (e.g. due to low utilization). At low utilization tools, arrival, maintenance and process time variability all get passed along to downstream tools as arrival process variability. For higher utilization tools, the departure process variability is essentially the variability from the process time and the equipment failures, which can still do a lot of damage.

I think that your idea of choosing the bottleneck to be a low variability tool makes a lot of sense. I've never heard of people explicitly doing this, but I have observed that tools like implanters often become cycle time bottlenecks even when they aren't strictly speaking bottlenecks in terms of utilization. In any case, as the spreadsheet that we presented last time illustrated, variability has the greatest impact on cycle time at high equipment loadings, so it would almost make sense to set your capacity buffers (for planning) according to the expected variability of the tools.

Your message overall has added to our motivation to explicitly add a capability like this to our company's cycle time management software enhancement list (we had been thinking about including coefficient of variation, but hadn't thought it through extensively). We currently track each lot move transaction, including move-in to queue, move-in to tool (start process), and move out (end process), so we have a fairly good base from which to calculate process time variability numbers. The most obvious way to do this seems to be to save the distribution of successive process times, and then calculate mean, variance, and coefficient of variation from this distribution. We would probably want to do this both by tool and by operation.

There is an extensive discussion of the different types of variability (from process time, downtime, setups, and rework) in the text Factory Physics, by Hopp and Spearman (see our review at www.FabTime.com/physics.htm), with formulas for computing the coefficient of variation and the squared coefficient of variation. The authors classify arrival process variability into three buckets: Low Variability systems have coefficient of variation less than .75, Moderate Variability systems have coefficients greater than .75 and less then 1.33, while High Variability systems have coefficient of variation greater than 1.33. We would probably use this classification for color-coding, so that it would be immediately clear from looking at a graph which tools or operations had high, medium, and low variability parameters.

In any event, we're thinking of including something like this in FabTime, and would

appreciate it if you could point us towards any other references on the subject, if you run across them. We will also share such references with our newsletter subscribers. Thank you again for such a detailed and thoughtful response to the newsletter.

### Characteristic Curve Generator

[Note, the latter section was updated slightly on 11/12/01, to reflect additional information received by FabTime.] Another reader asked: "I hope you could provide me the logic behind the formula:

CV = calculated system variation = Cs + (1+Cr)*RTR*(1-Av) (from the last newsletter issue)."

### FabTime response:

The revised formula (see issue 2.10 for an explanation) is

CV^2 = calculated system variation = Cs^2 + (1+Cr^2)*RTR*Av*(1-Av)

This formula was originally given to us by a colleague several years ago, someone with whom we have since lost touch. However, we obtained a slightly revised version from Mark Spearman, as included in the text Factory Physics, by Hopp and Spearman, Second Edition. The above equation may be found (with slightly different terminology) as Equation 8.6. We don't have the full derivation, but I can tell you my interpretation. It's an attempt to calculate an adjusted coefficient of variation, in which the process time variation is adjusted to also account for the variation due to random failures. This is a reasonable thing to do, since the downtime variability appears to the successive lots like variability in service time.

Here's how this ties to the formula: if there are no failures, then availability is 1, the whole second term drops off, and we're left with the service time variation only. (CV^2 = Cs^2 + 0).

If there are failures, then at a minimum (if the repair times are constant), the coefficient of variation is increased from Cs by a factor that's the product of RTR and PctDown. (CV^2 = Cs^2 + (1+0)RTR*Av*(1-Av)). RTR is that ratio of mean time to repair and mean process time. So, the larger the repair time is relative to the mean process time, the greater the increase in coefficient of variation. Similarly, the larger the percent down, the greater the increase in coefficient of variation. Both of these agree with my intuition about variability. Both the relative size of the downtime events (relative to process time) and the total amount of downtime affect variability, and hence estimates of cycle time.

This formula is only an approximation, but to me the logic behind it appears reasonable. The results that I get from the formula for relative effects due to repair time and service time variability, and overall percent downtime, agree with my intuition. This doesn't mean that you can use it to predict absolute values for average tool cycle times - only that it's a useful guide for looking at tradeoffs, in the form of characteristic curves.

## Setting Goals for Fab Performance

### Introduction

In a wafer fab, we use goals to interpret our absolute performance. If someone tells you "we did 125,000 moves today," you immediately ask yourself "is that good or bad?" Equivalently, "how close is that to our goal?" For every performance measure, there is likely a goal. Today we'll talk about setting goals, goal proliferation, and how we use goals.

But first, we need to discuss performance measures, and how the type of performance measure influences goal-setting. For some performance measures, there is a directional bias:

Scrap: Our goal is to decrease scrap, with the absolute best being zero scrap.
Cycle Time: Our goal is to decrease cycle times, with the absolute best being 1X theoretical (or you can argue that the absolute best cycle time is zero, since theoretical - raw process time - can be improved).

The performance measures from "The Goal" (throughput, operating expenses, inventory) fall into this directional category. We want to increase sales, and drive operating expenses and inventory toward zero. (For a book review of "The Goal" see www.fabtime.com/goal.htm.)

For other performance measures, such as moves (activities), there is no one absolute best number. The moves goal is determined by the configuration of the fab and the overall throughput goal.

Even when we know the absolute best performance (zero scrap, 1X theoretical cycle time) we may not choose it as our immediate goal. If current performance is far from the absolute best, it's probably easier to get there incrementally than in one large jump. E.g., the initial goal is 10% better than current performance, and when this goal is achieved, we aim for another 10% improvement. [Applied personally, I would love to shoot par at my local golf course. But that's a long way off, so my immediate goal is simply to reduce variability, e.g. the number of times I shoot worse than bogie.]

In today's discussion, we'll focus primarily on moves. However, I believe the ideas are relevant to other performance measures, too. (For a more detailed discussion of performance measures used in wafer fabs, see Issue 1.6.)

## Setting Moves Goals

At the highest level, you must start with a sales goal (equivalently, a sales forecast). The sales goal determines throughput numbers at various points in the supply chain, one of which is the fab. Most fabs will use their own capacity models to see if the throughput goals are feasible, and there may be a period of negotiation back and forth with the high-level planners. For foundries, where the downstream customer is not part of the same corporation, the process will be different, but it still requires sales goals and some amount of negotiation. No matter the process, eventually there will be a set of throughput goals for the fab, broken down by period and one or more levels of granularity (product family, technology, device type, device, etc.).

The fab then uses its line yield estimates to turn these throughput goals into a starts plan. With a starts plan, process flows, and step yield estimates, it is possible to directly calculate moves goals for individual operations (a capacity model will already be doing these calculations, in fact).

Let's look at a simple example. Suppose our fab makes two products A and B, with the following process flows. Yield is 100% unless indicated otherwise.

Process A: Op 10 (90% yield), Op 20, Op 30, Op 40.
Process B: Op 10 (90% yield), Op 20, Op 30, Op 20, Op 30, Op 40.

Let's assume we have already yielded our throughput numbers, to arrive at this starts plan:

A: 100 wafer starts per week (wspw).
B: 200 wafer starts per week (wspw).

If our demand is relatively smooth (this is a big assumption), and our starts are relatively smooth (another big assumption), and we have sufficient capacity throughout the line (yes, another assumption), then we can make the following estimates:
A: Op 10 (100 wspw), Op 20 (90 wspw), Op 30 (90 wspw), Op 40 (90 wspw).

B: Op 10 (200 wspw), Op 20 (180 wspw), Op 30 (180 wspw), Op 20 (180 wspw), Op 30 (180 wspw), Op 40 (180 wspw).

Rolling up the wafer-start numbers to the operation level, we get:

Op 10: 300 arriving wafers per week
Op 20: 450 arriving wafers per week
Op 30: 450 arriving wafers per week
Op 40: 270 arriving wafers per week

Thus, to keep up with arriving wafers, operation 20 has to move 450 wafers per week, while operation 40 only has to move 270 wafers per week. These become our aggregate operation-level moves goals. We can divide them by the number of shifts per week to transform them into operation-level moves by shift goals.

[Note: we have left rework out of our calculations here - in any real fab you would need to take rework into account when estimating moves goal based on a starts plan. The repeat visits to operations 20 and 30 for product B are not rework. They are applied to all lots, and are just an example of the normal reentrant nature of a wafer fab.]

## Goal Proliferation

Our example above was pretty simple. The result was four goal numbers, one for each operation. But even in this example, the goals can proliferate pretty quickly.

Suppose that the device manager for product B is concerned because the throughput for his product isn't meeting plan. He's probably going to want to look at moves by operation for his product. And he's going to want to compare these numbers against appropriate goals. In this case, it's straightforward to calculate these goals - the raw data is available from our discussion above:

Op 10: 200 arriving B wafers per week
Op 20: 360 arriving B wafers per week
Op 30: 360 arriving B wafers per week
Op 40: 180 arriving B wafers per week

And if we look at all goals, we have a table structure:

| Op | A | B | Total |
|---|---|---|---|
| 10 | 100 | 200 | 300 |
| 20 | 90 | 360 | 450 |
| 30 | 90 | 360 | 450 |
| 40 | 90 | 180 | 270 |

So instead of 4 goals (wafer moves goals for each operation), in practice we need to calculate and publish 12 goals (wafer moves goals for each operation, by product, and in total).

Taking lot owners into account (e.g. production, development, test, etc.) adds another dimension. Now instead of a goals table, we have a goals cube (imagine each operation/product entry in the above table broken into a goal for production wafers, for development wafers, and for test wafers). If there are three types of owners, then we need to calculate and publish 12 x 4 = 48 goals (the 12 shown above, plus 12 x 3 = 36 owner-level goals).

Suppose the fab has three priority classes: normal, hot, and hand-carry. Adding this priority dimension gives 48 x 4 = 192 goals.

To repeat: 192 goals.

That's quite a few, considering we only have two products and four operations. More realistically, even a small fab will have dozens of products and hundreds of operations. If our goal "cube" has four dimensions (operation, product, owner, and priority), it could easily contain 200 x 24 x 4 x 4 = 76,800 individual goals. Setting each one of these by hand is out of the question.

## Taking a Step Back

Do we need every entry in our goal cube? If we knew there were certain types of performance questions we would never ask, then we could leave sections of the cube blank. But we need to be careful, because that is just the time someone will say "Let's focus on our hot-lot R&D moves through photo for this new device, and make sure we are meeting our goals." With a complete goal cube, it's straightforward to roll up the entries to determine an appropriate goal for this performance measure. Otherwise, it's not easy. If you can limit the number of dimensions, that radically simplifies the cube. If you are not worried about tracking goals by lot owner, you don't need to include that dimension, and that makes the cube much smaller.

There are other ways to simplify the problem. For example, you may have rules regarding what percentage of lots are normal, hot, and hand-carry (90%, 8%, and 2%, say). Filling in the priority dimension of the goal cube, then, is a simple matter of multiplication.

And finally, we need to remember the assumptions we made earlier:

1) Demand is smooth
2) Starts are smooth
3) We have sufficient capacity

The goals we have focused on in this article are longer-term averages. If these three assumptions are not met in the short term, then it is quite likely that actual performance will not be anywhere near the goals, at least in the short run. Given the variability found in wafer fabs, you may be asking yourself "why do we need long-term goals?" They are necessary, however. Remember that these long-term goals are a result of the throughput plan. If we consistently fall short of these goals, then there's no way to meet the overall throughput goals.

However, it is appropriate to look at other goals in addition to these longer-term targets. For example, to address variability in WIP availability, you can look at turns (moves divided by WIP). To address equipment variability, you can look at utilization of available capacity. And ultimately, you could look at WIP distribution, equipment availability, and staffing, to arrive at a daily goal (for moves, say). This daily goal would vary from day to day, providing a short-term companion to the longer-term goals discussed above.

## Aside: Short-Term Goals

Calculating short-term goals based on current conditions (and measuring performance against these goals) is a very tedious manual task - much better to build an automated system. For these calculations, you need both real-time data, and a projection of where lots will move during the time horizon under consideration. Generating this projection is the tricky part. You can look at performance over the past few shifts and use statistical predictions. You can use a simulation model that's preloaded with current conditions. Or you can solve a simplified work-assignment problem (formulated as a mixed linear-integer programming problem). There are probably other techniques, but each has its own benefits and drawbacks. For our cycle time

management software, we are pursuing the first and third approaches. We also know of companies that have pursued the simulation approach.

### Summary

We are surrounded by performance measures. Goals help us to convert these absolute numbers into relative "good or bad" indicators. At higher levels of an organization, you deal with aggregated goals. More detailed goals must be set, however, at lower levels of the organization. These detailed goals must be consistent with the higher-level goals, and must be useful for day-to-day operations. The closer you look at the process, the more you see the proliferation of goals. If you can address this proliferation, you can generate appropriate goals for a wide variety of intermediate performance measures. It's important to remember the implicit assumptions behind long-term goals, however, and to mix long-term goals with appropriate short-term targets.

## FabTime Recommendations

### Thank You Image Gallery

As this newsletter has a large international readership, we wanted to point out a great website called the Thank You Image Gallery - International Responses to September 11th, at thankyou.fast-networks.net/index.cgi. The site contains pictures of the huge outpouring of international sympathy and solidarity displayed towards Americans at this difficult time. The site is rather slow to load, but worth the wait. The site is maintained by Ryan Garland.

### IC Knowledge

Court Skinner of SRC recommended this website to us (www.icknowledge.com). They have some interesting resources, including articles on the economics of wafer fabrication, a glossary of terms, and various other cost-related features. One feature article that we especially liked was a quick calculation that they did regarding just how bad 20% utilization is for a foundry, in terms of product cost ($3463/wafer, significantly more than the current average foundry pricing of $1,958 to $1,857). Another article suggests that for 300mm fabs, 40-50% utilization will be needed just to break even. We haven't looked into their calculations in detail, but we think that they are certainly exploring some good questions.

### Virus Myths

The recent Nimda virus has affected a number of our readers, and there are many excellent resources on both avoiding it and dealing it with it. But I've also noticed a number of email messages circulating about viruses that aren't true. These messages are a virus of sorts themselves, and so I refer you to the virus myths website (www.vmyths.com) for confirmation of questionable emails that you receive, and some guidelines for not being taken in regarding future myths.

### Woody's Watches

I learned of the Virus Myths website from an email newsletter called Woody's Office Watch that I've been reading regularly for years now. There are several different newsletters, on Office, Windows, Access, Project, and Palm Devices. All of them are free (they include some advertising in them). I've always found the information in the watches to be reliable, and they have sometimes helped me to avoid problems that I might have otherwise encountered (regarding patches, viruses, etc.). Though very focused on Microsoft products, the editors have a healthy skepticism regarding Microsoft (they are fully independent), and frequently entertaining. You can find them at www.woodyswatch.com.

# Subscriber List

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ICG / Semiconductor FabTech (1)
IDC (7)
Infineon Technologies (29)
Intarsia Corporation (1)
Integrated Device Technologies (1)
Integrated Technologies Company (2)
Intel Corporation (31)
Intelligent Quality Systems (1)
International Rectifier (1)
Intersil (2)
Interstar Technology (1)
IRIS Technologies (1)
James Nagel Associates (1)
JDS Uniphase (3)
Kansas State University (1)
Ken Rich Associates (1)
Lexmark International, Inc. (1)
Lockheed Martin Fairchild Systems (1)
LSI Logic (6)
Lynx Photonic Networks (1)
Macronix International Co. (3)
Managed Outsourcing, Inc. (2)
Maxim Integrated Products, Inc (3)
MEMS Optical (1)
Metrology Perspectives Group (1)
Micrel Semiconductor (1)
Microchip Technology (1)
Micron Technology, Inc. (1)

Micro Photonix Int. (1)
MicroVision-Engineering GmbH (1)
Motorola Corporation (36)
MTE Associates (1)
Multimedia University (1)
Nanyang Technological University (2)
National Semiconductor (12)
National University of Singapore (2)
NEC Electronics (6)
Nortel Networks (4)
Oklahoma State University (1)
ON Semiconductor (8)
Palmborg Associates, Inc. (2)
Penn State University (1)
Peter Wolters CMP Systeme (1)
Philips (13)
Planar Systems (2)
Powerex, Inc. (3)
PRI Automation (1)
Productivity Partners Ltd (1)
Propsys Brightriver (1)
Ramsey Associates (1)
Raytheon (1)
Read-Rite Corporation (2)
Redicon Metal
Rexam (1)
RTRON Corporation (2)
SAMES (1)
Samsung Semiconductor (2)
Seagate Technology (16)
SEMATECH (17)
Semiconductor Research Corp. (SRC) (1)
SEZ America, Inc. (1)
Shanghai Grace Semiconductor Mfg. (1)
SiGen Corporation (1)
Silicon Manufacturing Partners (3)
Silterra (M) Sdn. Bhd. (5)
Solectron Corporation (1)
SSMC (1)
STMicroelectronics (17)
Stonelake Ltd. (1)
Süss MicroTec AG (1)
Synergistic Applications, Inc. (1)
Synquest (2)
Takvorian Consulting (1)
TDK (1)
TECH Semiconductor Singapore (17)
TESLA SEZAM, a.s. (1)
Texas A&M University (1)
Texas Instruments (10)
Tokyo Electron Deutschland GmbH (1)
TriQuint Semiconductor (2)
Tru-Si Technologies (1)
Unisem (1)
United Microelectronics Corp (2)
University of Arkansas (1)
University of California - Berkeley (3)
University of Ireland - Galway (1)
University Porto (Portugal) (1)
University of Virginia (1)
University of Wuerzburg (Germany) (2)
Vasu Tech Ltd. (1)
Velocium (1)
Virginia Tech (1)
Wacker Siltronic AG (3)
Wacker Siltronic Corp. (1)
WaferTech (9)
Wright Williams & Kelly (9)
Xerox Brazil (1)
X-FAB Texas, Inc. (3)
Zarlink Semiconductor (6)
Zetek PLC (1)
Unlisted Companies (7)

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