FabTime Cycle Time Management Newsletter

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Information

Mission: To discuss issues relating to proactive wafer fab cycle time management.

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Welcome

Welcome to Volume 3, Number 4 of the FabTime Cycle Time Management Newsletter. This month's announcements include a conference/networking event, two newly available FabTime papers, and a newly available FabTime cycle time management course, developed for managers and supervisors. We are particularly pleased to announce this course to you, our newsletter subscribers, as the topics in the course reflect many of the topics that we have discussed here over the past two years. We would like to thank Steve Brown, of Medtronic Microelectronics Center, and Dan Siems, of Philips Semiconductors, for their feedback regarding the course objectives and topics. Steve, in fact, encouraged us to take the course from an idea for "someday" to a reality. This month in the subscriber discussion forum we have several responses to last month's main topic of equipment dedication. Other topics discussed in this issue include lot size change, foundry performance data, and the interaction of AMHS control and dispatching.

This month's main article, Cycle Time and the Core Conflict, is a guest article, written by Dan Siems, of Philips. Dan was recently appointed World Wide Wafer Fab Cycle Time Manager for Philips Semiconductors. This article represents Dan's thoughts on a core conflict that often exists in managing wafer fabs - trying to get lots out quickly, but having to frequently stop the lots for quality checks. Dan proposes the elements that he believes must exist to weaken this conflict, and maintain good cycle times over the long term. I think that his ideas will stand Dan in good stead as he begins his new position for Philips, and I think that our newsletter audience can benefit from the ideas, too.

Thanks for reading! -- Jennifer

FabTime

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Community News/Announcements

New Cycle Time Management Course Available from FabTime

FabTime is pleased to announce the availability of a new two-day course on cycle time management. The purpose of the course is to provide production personnel with a more in-depth understanding of the issues that cause cycle time problems in a fab, and to suggest several possible approaches for improving cycle times. The material in the course is drawn from, and expands upon, ideas described in this newsletter and on FabTime's website. The course was developed for managers and supervisors. (A separate course for industrial engineers, focusing more on the technical details, may be available in the future.) Course topics include: Building intuition with basic queuing models; choosing an appropriate cycle time management style; resolving data issues; and calculating metrics and goals. Hands-on exercises are used throughout. If you would like Frank or Jennifer to visit your site to present this course, please email Jennifer.Robinson@FabTime.com

New Papers Available from FabTime's Website

Two new papers are now available from FabTime's website. The first describes a procedure developed by AMD for super-expediting hot lots. This paper, by Mike Hillis from AMD and Jennifer Robinson from FabTime, was presented at the MASM 2002 Conference in Phoenix on April 11th. The abstract was included in last month's newsletter, and can now be found at www.FabTime.com/abs_MASM02.htm. The second paper, by Jennifer Robinson, will be published in the April issue of Semiconductor FabTech. The abstract is included below, and can also be found at www.FabTime.com/abs_FabTech02.htm.

Abstract: There are many good reasons to improve wafer fab cycle time. Lower cycle times allow for faster product development cycles, and speedier time to market for new products. Lower cycle times also allow companies to maintain lower inventory levels, and to better satisfy customers. Some studies have shown a correlation between reduced cycle times and improved line yield (a clear dollar benefit). All in all, improving cycle times can improve both customer satisfaction and the semiconductor manufacturer's bottom line. The first step to improving cycle times is to understand the factors that make wafer fab cycle times high in the first place. In this article, we will first discuss contributors to wafer fab cycle times, and then propose some suggestions for making low-cost improvements.

Both of these papers can be requested from FabTime's website by using the form at http://www.FabTime.com/request.htm.

OpVent 2002

Dr. Ingo Hussla of IZET wrote: "We would be happy if you could announce OpVent 2002, a business & opportunity matchmaking event right after Semicon Europe, 19th of April 2002 here in Itzehoe/Hamburg. We are organizing a tour of Fraunhofer/Vishay facilities. Please check www.opvent.com."

FabTime welcomes the opportunity to publish community news and announcements. Simply send them to Jennifer.Robinson@FabTime.com.

Subscriber Discussion Forum

Issue 3.03 - Tool Dedication

A long-time subscriber wrote: "Interesting newsletter, as always. I find it useful even though I don't work directly in wafer fabrication. The method of approximating the effect of tool dedication was especially fascinating and useful...here at my company, even though our machines are organized and located by type, we've still long had this concept of "virtual production lines" where we'll allocate one or more "lines" to each product we make and operate them as strict production lines--even though other products use the identical process at some steps and could be run interchangeably on machines outside their "lines." I know that abandoning this policy in favor of open production would improve capacity and/or cycle time, but I've met with some resistance (because an advantage of virtual production lines is better lot integrity, which speeds up failure analysis and trouble-shooting). So the estimated quantitative effect of the Sakasegawa method could be a good sales tool."

Joe Wadsworth, Editor of Semiconductor FabTech, wrote: "Your example of queuing in everyday life uses supermarkets and says that it is unlikely that we will see 'single line - multiple servers'. I don't know if I'm the first to tell you, but in central London, we have a brand called Sainsbury's, who have embraced this wholeheartedly for their 'local' stores, which cater mostly for shoppers looking to make small daily purchases (lunch!). Maximum throughput is their game, and consequently we are all herded into a line, which moves (at quite some pace I can tell you) until you get to the front and are then designated a cashier.

It works quite effectively; no longer do you worry if you are standing behind someone with thousands of reduced items (you know the ones that require stickers removed, manual typing of barcode, individual weighing of fifteen different types of fruit - that sort of thing), and you get more people to talk to or watch. You start to notice there are 'hot' tills and the bogus tills staffed by a newbie that must be avoided at all costs and thus necessitate a stall maneuver usually involving inspection of bananas. ("Oh these look nice - do go ahead of me.....")"

FabTime Response:

Joe showed us that we shouldn't assume that something hasn't been done, just because we've never seen it. We think that it's great that Sainsbury's has been smart enough to try this, and that it works well in practice.

Rick Alexander of AMI Semiconductor wrote: "Sometimes it makes sense to dedicate tools in relationship with lowering cycle time and increasing OEE. One such example would be photo cluster tools in the photo lithography area, in a Fab that manufactures a wide variety of processes and products. Suppose your photo area has 10 cluster tools that have an average expected throughput (EUPH) of 65 wafers per hour for a total output of 650 UPH. If all the photo clusters are allowed to process all material including (special processing, engineering lots, engineering experiments, development lots, priority lots, and lots with device specific processing) the average UPH per tool drops to 50 wafers per hour for a total output of 500 UPH. Special processing has a huge impact on the cluster tools, and increases Idle Time and Setup losses. Now, if you dedicate 2 photo clusters to handle all of the special processing requirements, the two clusters UPH numbers drops to 10 wafers per hour per tool for a total of 20 UPH. The other 8

clusters can be utilized to handle the normal material at an average UPH of 65, for a total of 520 UPH. By dedicating 2 photo clusters to handle all of the special processing requirements, the UPH for the photo area increases from 500 to 540 wafers. The bottom line is you have to take into account the start mix and different process variables in your line before deciding to dedicate specific tools."

FabTime Response:
We think that Rick makes an excellent point about setup and idle time losses on cluster tools, and in favor of tool dedication in certain specific situations. Rick's numeric example is particularly helpful in showing exactly what he means.

Foundry Performance Data

Bob Kotcher (MMC Technology) wrote: "In answer to Toby Patterson's query, U.C. Berkeley's Competitive Semiconductor Manufacturing Program conducted a detailed analysis of many fabs around the world and compared many performance parameters, including yield and cycle time. Some of the analyses are several years old but I still find them quite interesting. They are available--many at no cost--at: http://esrc.berkeley.edu/csm/."

AMHS <- -> Lot Dispatching

Another subscriber wrote: "I have a question that deals with AMHS <-> Lot Dispatching:

Do you know any papers that deal with coupling material control of AMHS with lot dispatching in the 200mm area? Or do you know anybody (IT or Automation manager etc.) from a waferfab equipped with an AMHS for interbay transportation and a lot dispatching system (preferably Brooks RTD)?

I have some colleagues and also customers who want to discuss some ideas and interchange experience if there is any benefit to couple transportation control software (MCS) and lot dispatching software for 200mm fabs (not fully automated). I think in the 300mm area with intrabay automation there is definitely a need to establish a communication between material control and lot dispatching. However, I have no ideas how this looks like in 200mm fabs with interbay systems and manual machine loading."

FabTime Response:
I only know of two papers on this topic (references below):

J. T. Lin, F.-K. Wang, and P.-Y. Yung, "Simulation Analysis of Dispatching Rules for an Automated Interbay Material Handling System in Wafer Fabrication," *International Journal of Production Research*, Vol. 39, No. 6, 1221-1238, 2001.

T. Arzt and F. Bulcke, "A New Low Cost Approach in 200 mm and 300 mm AMHS." *Semiconductor FabTech, Tenth Edition*, ICG Publishing, 1999.

Nor do I know off the top of my head whether people are doing as you describe in their 200mm fabs. I do know of some people who are using RTD for dispatching, but I don't know whether or not they have an AMHS for interbay transportation in those fabs, or what they do for communicating between the RTD and AMHS systems. Therefore, I am including this question in the newsletter, to see if any readers are interested in exchanging ideas on this topic. If so, please write to Jennifer.Robinson@FabTime.com, and I can put you in contact with the person who raised this question.

Lot Size Change

Youssef Benmokhtar of ST Microelectronics asked: "I had a question regarding lot size and its impact on CT. In a previous

issue of your newsletter, you discussed the advantages of smaller lot sizes. In the fab I work in now, we are thinking about switching from a batch size of 50 to 25 (standard in the industry). Based on your article, the benefits on CT are obvious, but some factors may detract from reducing CT. Could you give me contact names of companies or fabs that have been through such a change successfully or not."

FabTime Response:

For the one fab that we know that seriously considered, and rejected, changing the lot size from 50 to 25, the capacity of the material handling system (for smaller, more numerous lots) was the primary sticking point.

We don't know of any real success stories in the area, so we are posing the question to our newsletter community. If you have been through a lot size conversion in your fab, or have considered making such a conversion and decided not to, and you would like to discuss it, please let us know. We can put you in touch with Youssef, and, if you wish, publish your observations in a future newsletter issue. Thanks!

Cycle Time and The Core Conflict - by Dan Siems

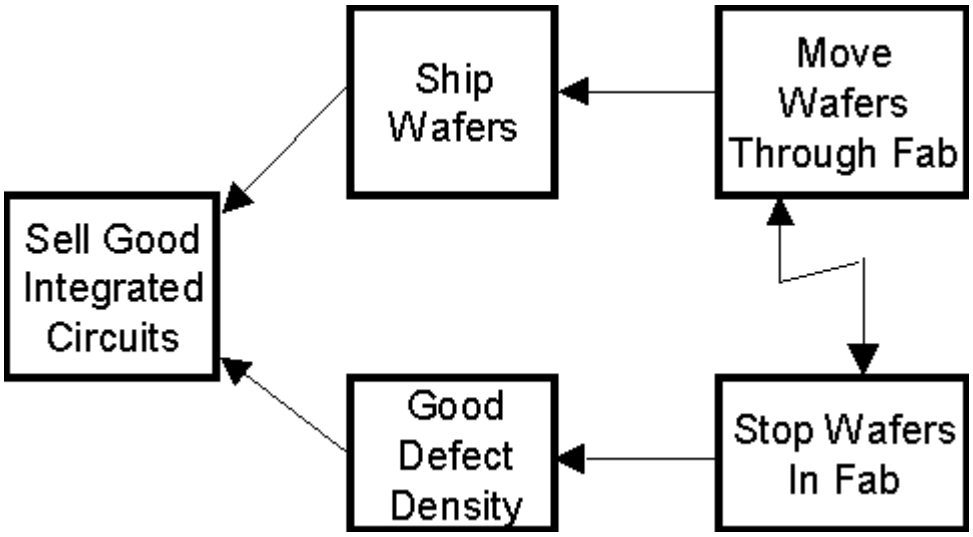
Introduction

A core conflict (1) is something within an organization that generates undesirable behaviors. We observe, work around, and participate in these behaviors that result from the core conflict - a conflict that comes from our best efforts and rests on certain assumptions. We use these assumptions to navigate and make sense of our work. Sometimes these assumptions - called mental models, grids or paradigms - remain unchallenged even when the context with which they were derived changes.

The core conflict lives because we get good at working within it - this skilled incompetence (2) becomes valued by the organization - often driving the conflict underground. Confronting the organizational tug-of-war and the resulting distractions often generates more heat than light.

The cloud (3) shown on the next page diagrams a classic core conflict found in many wafer fabs:

(It is best to read a cloud from left to right.) Begin with the objective: sell good integrated circuits (at a profit). To do this we need to ship wafers and have good defect densities. To ship wafers we must move wafers through the process in the fab. To achieve good defect density we must 'stop' wafers in the fab - wafer inspections, tool cleans, PM's, quals, measurements, reworks, tool restrictions, special routings - all activities associated with controlling variation. There is a conflict between moving wafers and stopping wafers, represented by the zigzag arrow. This core conflict generates an array of undesirable effects, some of which are: compromise, guessing, shortcuts, and under-specification of expectations - all resulting in poor decisions, mythical learning and lost time. The clock continues



to tick regardless of these distractions - and cycle time increases. Look at the hold lot list at any given moment for clues to the existence of your core conflict related to special causes. Metrology queue times give clues to your core conflict in light of common cause variation.

Traditional Intervention Methods

We often (but not always) organize around the conflict - like a tug-of-war - in this case manufacturing taking one side and process engineering taking the other. Efforts to improve cycle time appear to favor only one side of the conflict - quantity. Resistance builds from the other side - quality. Both sides hide behind the other when performance metrics fails to meet expectations.

One intervention into this core conflict is to reorganize - move accountability from quantity or quality, to quantity + quality. In this instance make an individual responsible for manufacturing, maintenance, and engineering for a specific part of the process. Under the right leadership, this reorganization works . . . for a while. However, due to specific local-area measures that must be in place to assure quantity + quality, sub-optimization results at the expense of another part of the line. For example, the CMP area **could** make wafers flatter and thereby improve the throughput in lithography, but this slows CMP down - besides, "the wafers are flat enough" or "flatter than most". CMP quality and quantity metrics become satisfied, yet the fab's bottleneck - lithography - suffers for it. Cycle time as a local metric could result in an overall **increase** in fab cycle time!

The core conflict can involve anything - generally, in manufacturing it involves cost, throughput and quality. As you will see in a moment, cycle time improvement efforts will not stick unless attention is given to weakening the core conflict. Reflective question: All of our fab managers know how to improve cycle time, why isn't it done?

A Theory of Constraints-Based Approach

Eli Goldratt proposes the Theory of Constraints as a guiding thought toward lasting change. Under-girding 'Drum, Buffer, Rope', Bottleneck Management, Critical Chain and other applications of TOC are the 'Thinking Processes'. The Thinking Processes require a disciplined, rational and highly logical approach to change, demanding both patience and endurance. Distractions of running wafer fabs often prove too much for a proper

engagement into the Thinking Processes, yet this is exactly where we should go to design an effective intervention.

I am suggesting that an effective intervention is dependent on both a Technical Solution AND a Change In Thinking to create sustained cycle time improvement gains. The technical solution brings all of our science to bear in running a wafer fab - variation reduction, inventory control, capacity expansion, TPM, etc. A Change in Thinking addresses the core conflict and implements the technical solution.

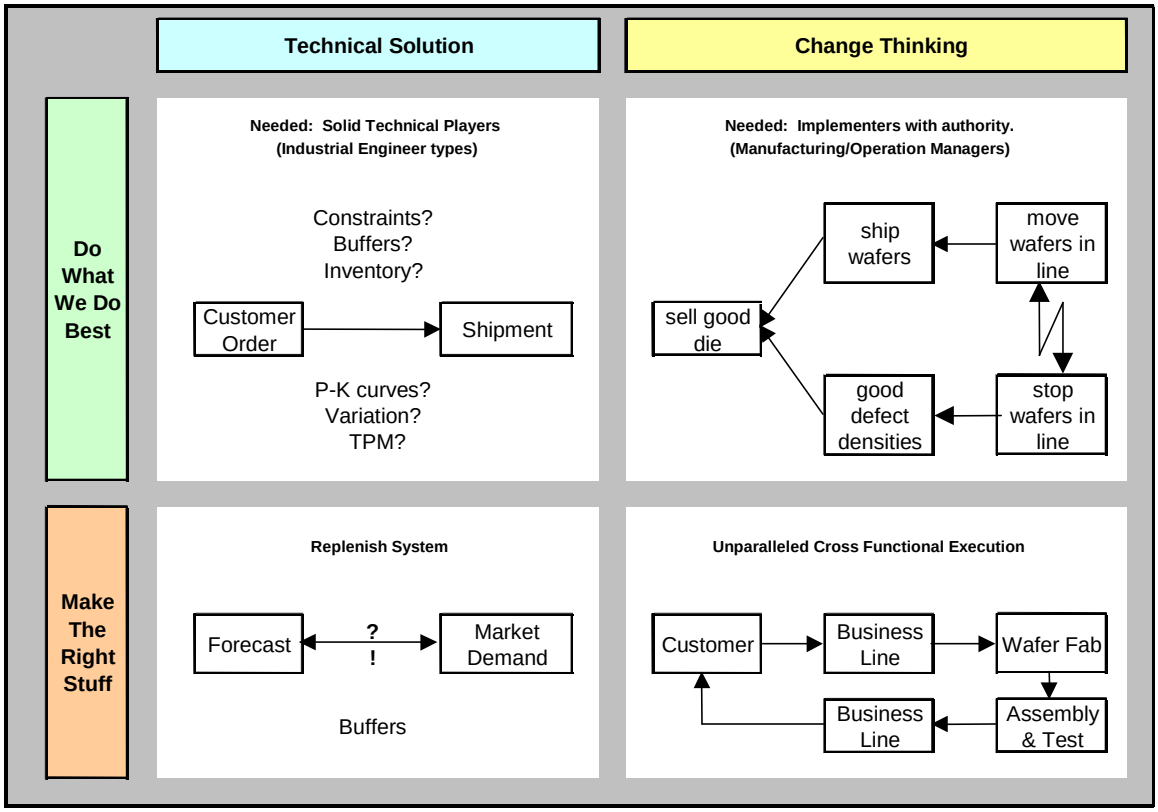
The following glyph illustrates four quadrants (4) of our cycle time battle.

Down the side: **Do What We Do Best** (i.e. make good integrated circuits), followed by **Make The Right Stuff** (i.e. make the right integrated circuits at the right time - I am not addressing this today). Across the top of the table: the **Technical Solution** and **Change Thinking**. We often concern ourselves with the first quadrant - which is necessary but not sufficient (5) to successful cycle time reduction. The Technical Solution will bring insight to our thinking but will not affect our behavior unless the core conflict is dealt with during implementation.

Actions to weaken the core conflict (**Change Thinking**) will be unique to each wafer fab because each fab is made up of unique individuals - even if there are common metrics across these fabs. Given the uniqueness of each solution to cycle time improvement the question then becomes: What **method** will lead to <u>your</u> solution? I believe the method involves three elements - the Thinking Processes (6), technical savvy (7), and teachable people to get it done.

Conclusions

The Technical Solution involves capacity modeling based in reality, a system for eliminating equipment/process variation and a method of managing work in process (8) - all using a guiding theory that is acted



on. Changed Thinking requires leadership with a desire to see the core conflict weakened and a thirst for fast cycle time - they should have the authority to subordinate the organization to a goal. This leadership also needs to be able to teach - not necessarily in the strictest sense - but through coaching, expectation setting and reinforcement. They should have the charisma to guide the organization to implement the technical solution in achieving fast cycle time.

Next Steps

So what's a fab manager to do next? Several well-known quotes come to mind:

■ "It depends." (9) Uniqueness lies within organizational boundaries – often generated by upper management personalities. Remember: your solution is your solution. This type of solution cannot be copied from one location to another – but the method of arriving at the solution can. Goldratt suggests a method called the Thinking Processes. Go there first, because the first thing done is analyzing the current reality – core conflict – followed by designing the future reality (the solution) with an implementation strategy.

■ "Just Do It." (10) and "Boldly go where no one has gone before." (11) Effort and perseverance are required. The key words are GO and DO.

■ "Is It In You?" (12) This intervention cannot be delegated – YOU must do it.

This article raises more questions than it answers – I hope you set out on the path toward lasting cycle time improvement in search of the answers.

Notes

(1) Avraham Y. Goldratt Institute: *Field Guide to the Theory of Constraints Thinking Processes*. p1.29, ©2000 Avraham Y. Goldratt Institute, 442 Orange Street, New Haven, CT 06511, (203)624-9026.

(2) Chris Argyris, *Overcoming Organizational Defenses: Facilitating Organizational Learning*, p.12, ©1990 by Prentice Hall, Inc. Upper Saddle River, New Jersey 07458.

(3) Eliyahu Goldratt and Jeff Cox, *The Goal: Second Rev*, ©1992, North River Press.

(4) Thanks to Tracey Burton-Houle and Hugh Cole - associates of Avraham Y. Goldratt Institute - for this enlightening discussion, 22-Mar-2002.

(5) Eliyahu M. Goldratt, Eliyakim Schragenheim, and Carol Ptak, *Necessary But Not Sufficient*, ©2000, North River Press.

(6) For example, as outlined by the Avraham Y. Goldratt Institute (www.goldratt.com/sclice.htm).

(7) For example, as explained by FabTime (www.fabtime.com).

(8) Thanks to Venkat Thupakula, Philips Semiconductors, for several discussions revolving around the proverb, "In all labor there is profit, But mere talk leads only to poverty."

(9) Thanks to Dr. Richard Post, of Dr. Richard Post and Associates. He always gave this answer. It worked.

(10) Nike ad slogan.

(11) James T. Kirk – StarTrek.

(12) Gatorade ad slogan.

Author Information

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FabTime Recommendations

Infotrieve Website

We have recommended other websites in the past that allow users to search among journal and proceedings abstracts. Infotrieve allows you to search abstracts and tables of contents from a wide array of journals and conference proceedings, and also includes MEDLINE searches (MEDLINE is the definitive repository for medical articles). The query engine is fast and powerful, and the user interface is easy to understand. What makes Infotrieve particularly useful, however, is the fact that if you find an article that you want, Infotrieve will deliver it to you (electronically or by mail or fax). Not all articles are currently available for electronic delivery, but many are. The company charges a fee per article, usually consisting of a $12 delivery fee plus a copyright fee. The copyright fees vary, but seem to be on the order of $10 to $25. Considerably more expensive than going to the library to copy the article, but also a lot easier, and you don't have to worry about violating anyone's copyright. You can find Infotrieve at www4.infotrieve.com/.

Librarians' Index to the Internet

The Librarian's Index to the Internet is just what it sounds like. A categorized directory of useful websites, with ratings and descriptions of all of the sites. Their about page says: "Our motto: "Information You Can Trust." The Librarians' Index to the Internet (LII) is a searchable, annotated subject directory of more than 9,000 Internet resources selected and evaluated by librarians for their usefulness to users of public libraries. LII is used by both librarians and the general public as a reliable and efficient guide to Internet resources." This site was recently recommended by Inc Magazine, and FabTime recommends it too. You can find it at www.lii.org/. They also have a free newsletter that you can sign up for, with which they send you links to the best newly added sites every week.

Web-Surfer-Friendly Hotels

Using the LII (described above), I found a website called GeekTools, maintained by "the guys at CenterGate® Research Group, LLC". The website includes links to software applications, calculators, etc., including a variety of things that I found rather cryptic. But one thing that I found immediately useful was a page called Geektels. Geektels are geek-friendly hotels, in terms of their high-speed internet access availability. Now, I don't think that our FabTime newsletter community qualifies as geeks, just because we work in the high-tech industry. But I would guess that a very high percentage of us could appreciate hotels with high-speed internet access. Geektels has a simple, drill-down interface (country/state/city), and lists the number of hotels available in each category. If you have a trip coming up, you can use this website to see if it's worth dragging your Ethernet cable along. You can find this website at whois.geektools.com.

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FabTime (3)
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MASA Group (1)
Maxim Integrated Products, Inc. (3)
MMC Technology (1)
MECA Electronics, Inc. (1)
Medtronic (5)
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Methode Electronics, Inc, (1)
Metrology Perspectives Group (1)
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Microchip Technology (1)
Micron Technology, Inc. (1)
MicroVision-Engineering GmbH (1)
Mitsubishi Semiconductor Europe (1)
Motorola Corporation (44)
MTE Associates (1)
Nanometrics (2)
Nanyang Technological University (3)
National Chiao Tung University (1)
National Semiconductor (12)
National Univ. of Ireland - Galway (1)
National University of Singapore (2)
NEC Electronics (7)
Nortel Networks (7)
Ohio State University (1)
Oklahoma State University (1)
ON Semiconductor (8)
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University of Texas at Austin (1)
University of Virginia (1)
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Virginia Tech (7)
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Wacker Siltronic (3)
WaferTech (11)
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Zarlink Semiconductor (2)
Zetek PLC (1)
Unlisted Companies (15)

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