FabTime Cycle Time Management Newsletter

Volume 8, No. 6 July 2007

Information

Mission: To discuss issues relating to proactive wafer fab cycle time management

Publisher: FabTime Inc. FabTime sells cycle time management software for wafer fab managers. New features in the software this month include PriorityClass/HoldTime and PriorityClass/ProcessTime alerts, which allow users to be notified if any lot within a particular priority class remains on hold or in process longer than a specified limit.

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Welcome

Welcome to Volume 8, Number 6 of the FabTime Cycle Time Management Newsletter! In our community news section, we summarize information about four upcoming conferences that have relevance for fab manufacturing performance improvement. Our FabTime software tip of the month is about restricting FabTime data access for individual users. We also have a subscriber discussion topic, introduced by Walt Trybula, related to last month's question about fab utilization.

This month's main article was written by Professor Scott Mason of the University of Arkansas, a national expert on dispatching, scheduling and manufacturing performance improvement for wafer fabs. Frank and I have worked with Scott since our days at Sematech in the early 1990's, and we are pleased to welcome him as a contributing writer to the newsletter. We anticipate working with him on future articles and other projects. This month, Professor Mason addresses cluster tools. He provides an overview of cluster tools, including a discussion of some of their pros and cons, and then discuss approaches (both academic and practical) for modeling and analyzing cluster tools in order to develop estimates of tool capacity and cycle time. He also shows, by example, the way that adding a chamber can sometimes increase capacity, while decreasing cycle time, for a cluster tool, by reducing blocking. We hope that you will find this article of interest, and we welcome your feedback.

Thanks for reading!—Jennifer

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Community News/Announcements

Upcoming Industry Conferences

There are several upcoming industry conferences focused (some in part) on manufacturing performance improvement for wafer fabs.

■ The 4th ISMI Symposium on Manufacturing Effectiveness will be held October 24th and 25th in Austin, Texas. According to the conference website (http://ismi.sematech.org/ismisymposium/), "This year's Symposium emphasizes "productivity in depth"—with exclusive data to enhance your engineering knowledge and bring cutting-edge benefits to your company's bottom line. Experts will share information and methodologies for reducing manufacturing expenses in both existing and next-generation fabs through advances in equipment, process, resources, fab design, and manufacturing methods. Challenges will be addressed in several parallel sessions dealing with fab and equipment productivity, ESH, fab design, defect inspection, statistical methods, modeling and simulation, e-manufacturing, and lean manufacturing."

■ The 3rd International Conference on Modeling and Analysis of Semiconductor Manufacturing (MASM 2007) will be held in Scottsdale, Arizona on September 22nd to 25th, as part of the 3rd annual IEEE Conference on Automation Science and Engineering (IEEE CASE 2007). You can find more information in this announcement and call for papers: http://www.fulton.asu.edu/~case2007/downloads/CFP_IEEE_CASE2007_MASM.pdf. The announcement says that "MASM 2007 will again be a forum for the exchange of ideas and best practices between researchers and practitioners from around the world involved in modeling and analysis of semiconductor manufacturing. We are interested in any methodologies, research, and/or applications from other industries, as well, that might also be utilized for the semiconductor industry".

■ The 16th International Symposium on Semiconductor Manufacturing (ISSM 2007) will be held October 15th to 17th in Santa Clara, CA. According to the conference website (http://www.issm.com/), "Founded in 1992, ISSM is the industry's largest assembly of semiconductor manufacturing professionals dedicated to driving technology innovation and operational excellence within the industry. Currently, ISSM alternates between the US and Japan with the goal of providing an open global forum for the introduction and promotion of new concepts to advance semiconductor manufacturing."

■ The 2007 Winter Simulation Conference will be held in Washington, DC from December 9th to 12th. The conference focuses on all aspects of discrete event simulation, and features a semiconductor manufacturing track with emphasis on operational policies and system configurations. More details are available at http://www.wintersim.org/.

FabTime welcomes the opportunity to publish community announcements. Send them to newsletter@FabTime.com.

FabTime User Tip of the Month

Restrict Data Access for Individual Users

Do you have specific sub-sets of FabTime data that you would like to be able to share with particular users? For example, would you like to be able to show shipment or cycle time data for their own products to internal customers? We have recently added this functionality to FabTime, though it must be configured by your site's FabTime administrator. For any user account, you can enter an override for the QueryString that is sent to all the chart procedures. In that case, it doesn't matter what the user enters on a chart, the override always takes precedence. To do this:

1. Log in to FabTime using the "administrator" account.

2. Click "User" in the red toolbar, to go to the user setup page.

3. Add a new user (with the "new user" link), or select "edit" for an existing user.

4. From the user detail screen, enter your desired data restriction in the "Filter/QueryString Override" box. For example, to restrict WIP charts to only display Flow abc, enter "FlowsLike=abc". Combine multiple filters with &, e.g. "FlowsLike=abc&LotsLike=F1*". Use "FactoryID=x" to limit users to a particular factory, e.g. "FactoryID=1&FlowsLike=abc".

In combination with the above, you will probably want to also limit the charts that this account has access to – you can do that with the "Restrict to specific chart?" box. For example, you may want to limit a particular user to see the lot history chart and the moves lot list chart. When that user logs in and goes to the charts page, he or she will see only the charts that you select here. Note that if you allow a user to use the lot progress chart (where it shows history + projected steps), you should use a QueryString override that references the lot name or the flow name.

If you have any questions about this feature (or any other software-related issues), just use the Feedback form in the software.

Subscriber Discussion Forum

Issue 8.05: Fab Utilization

Walt Trybula (The Trybula Foundation and Texas State University – San Marcos) and submitted the following additional question, in response to last month's subscriber discussion question about fab utilization from **Dov Kotlar** (Tower Semiconductor. "Interesting published conversation with Dov. While I have strong opinions of how things should be measured, I have a question that points out some of the differences in view. (By the way, the level of management interested in the measurement determines the type of measurement that is important.) Consider a single wafer fab built with existing equipment. Thermal processing is still a batch operation. However, it is starved until it obtains 50 or 100 wafers. According to many measurement approaches, it is not a bottleneck because it is starved. In reality it is a bottleneck due to needing the full load. Do we not have similar situations in the existing fabs? I am leaving this as an

open question to provide some food-for-thought."

FabTime Response: Readers, what do you have to say about Walt's point? Is the batch tool that you hold idle to run with a fuller load a bottleneck?

P.S. For those interested, you can read more about Walt's current efforts at Texas State, and see a photo of him in his cowboy hat, here: http://www.txstate.edu-/rising-stars/walt-trybula.html.

Cluster Tools in Wafer Fabs

Written by **Professor Scott Mason** (University of Arkansas

In this article we discuss an important type of fab processing tool that continues to gain acceptance and use in wafer fabs: cluster tools. Below, we will provide an overview of cluster tools, including a discussion of some of their pros and cons, and then discuss approaches (both academic and practical) for modeling and analyzing cluster tools in order to develop estimates of tool capacity and cycle time.

Background

For many years, the individual process steps required to fabricate integrated circuits on a silicon wafer were performed on a number of individual tools. For example, a typical photolithography "loop" consisting of coat, expose, and develop processing steps was performed by three different fab tools: a coater, a photolithography stepper, and a developer. Subsequent equipment engineering developments resulted in the development of integrated coater and stepper "tracks" that linked these two processing steps together. Using this type of inline arrangement, increased tool throughput could be achieved by maintaining a proper, consistent flow of wafers to the stepper.

As silicon wafer substrate sizes increased from 150 to 200 mm, and then to 300 mm in diameter, device geometries correspondingly decreased from 0.5 to 0.25, to now 0.18 microns and below. These two factors combined to further complicate manufacturing process requirements for fabricating semiconductors. As a result, tools continued to increase both in footprint (square feet of fab area occupied) and processing capabilities. Perhaps borrowing on earlier experience and success with integrated photolithography processing tools, new, multi-functional "cluster" tools comprised of a number of configurable processing "chambers" surrounding a central robotic handling unit began to gain acceptance in the semiconductor industry. Cluster tools were a cost effective means of reducing fab footprint requirements while simultaneously processing wafers through a number of sequential processing steps.

Srinivasan (1998) effectively defines a cluster tool as "an integrated, environmentally isolated manufacturing system consisting of process, transport, and cassette modules mechanically linked together." Consider a hub and spoke arrangement similar to that of a bicycle

wheel. Integration is achieved through the clustering of a number of different chambers which act as spokes, surrounding the hub which contains the wafer handling robots. Each chamber typically processes a single wafer at a time, with the robotic handlers being responsible for moving wafers between chambers in a predefined sequence or order. Both Zuberek (2004) and Lee and Lee (2006) investigate recent processing developments wherein a chamber is revisited during normal processing through a cluster tool (i.e., recirculating or re-entrant flow within a cluster tool. Environmental isolation is achieved when a lot of some number of wafers is loaded on the cluster tool via a load lock. Once a cassette of wafers is loaded, the load lock typically pumps down the atmosphere surrounding the wafers to match the environment contained within the cluster tool.

Advantages associated with incorporating cluster tools into a wafer fab can include increased wafer yield due to reduced contamination, increased throughput/shorter product cycle times as compared to processing wafers on individual tools, better floor space utilization, and reduced requirements for human intervention. In addition, chamber configuration is flexible, as manufacturers that initially purchase some set of processing chambers often add on to and/or reconfigure their cluster tool when demand and/or processing requirements change. However, the failure of a single processing chamber can cause an entire cluster tool to be down, as the linked set of processing steps performed by the cluster tool often cannot be completed when a chamber fails.

Cluster tool reliability is a function of how tool chambers are configured. Zuberek (2004) describes chamber configurations as serial, parallel, or hybrid. In a serial configuration, a wafer is required to visit each chamber in the cluster tool during its processing. Parallel-configured cluster tools have multiple chambers capable of performing a given process step. In this way, tool reliability can be improved as the failure of a single chamber will not render the tool completely down, except in the case when all chambers of a given type/process are failed. Zuberek (2004) states that while parallel configurations are better from a reliability standpoint, serial configurations provide higher throughputs. The hybrid cluster tool configuration results when a cluster tool contains only one chamber of a certain type (e.g., clean), but multiple chambers of another type (e.g., deposition).

Cluster tools can be configured in an almost countless number of ways, considering the fact that semiconductor manufacturers can order cluster tools from equipment suppliers with a number of different chambers (typically between two and four) with varying processing capabilities (for example, cleaning, etching, or deposition). Further, chambers in a cluster tool may all be unique, or contain multiple copies of a given chamber type. Finally, different robotic handling options (typically one or two robot units) are available for purchase, along with different load lock configurations (typically, single (one lot at a time) or parallel (two lots at a time)).

This ultimate flexibility or configurability afforded by cluster tools is the primary reason that estimating the capacity and/or throughput performance of a cluster tool is a challenging endeavor. Considering the fact that fab capacity depends on what mix of products is being manufactured, it follows that cluster tool capacity depends not only on product mix, but also on the number of and types of chambers present, robotic wafer handling capabilities, and wafer input rate as dictated by load lock configuration. With this in mind, we now turn our focus to analysis techniques and models for analyzing cluster tool performance.

Modeling and Analyzing Cluster Tool Performance

In the academic literature, a number of authors have written papers that analyze and/or schedule cluster tools with the goal of maximizing tool throughput. As the configuration of a cluster tool, along with other factors described above, directly impacts a cluster tool's capacity or throughput capability, a variety of analysis techniques have been examined in the literature, including Petri nets (see Srinivasan (1998) and Zuberek (2004)), metaheuristics such as simulated annealing (see Yim and Lee (1999)), mathematical optimization (see Lee and Lee (2006)), or discrete event simulation. These approaches are typically used to estimate cluster tool throughput and/or cycle time capabilities, as well as to investigate the potential for blocking and/or deadlock to occur within the cluster tool.

Blocking occurs when a wafer has completed its required processing in its current chamber, but cannot be moved to its next process step as the destination chamber is occupied/full. In addition to blocking, another undesirable outcome of cluster tool operations is deadlock. Deadlock occurs when two or more competing actions are waiting for each other to finish, and therefore, nothing ever finishes. For example, consider two chambers named "A" and "B." Assume the wafer in chamber "A" has completed its processing and is destined for chamber "B." Deadlock can occur if the wafer currently in "B" is destined for "A" once its processing in "B" has completed. This problem can become a reality when multiple lots are processed on a cluster tool that contains only a single robotic handler.

While additional references are provided at the end of this article for the reader's reference, we now focus on two more practically relevant methods for analyzing cluster tool configuration performance: static (spreadsheet) analysis and dynamic (simulation) analysis.

Static, Deterministic (Spreadsheet) Analysis

In practice, cluster tool analysis often is performed by static, deterministic analysis via spreadsheet. In static analyses, manual calculations are performed for wafer start and ending times within each chamber. In this approach, the processing time required in each chamber is used along with some basic mathematics to understand how wafers travel throughout the cluster tool, when blocking and/or deadlock occurs within the tool, and how/when wafers will exit the tool.

Consider a lot of six wafers that must be processed through a three chamber cluster tool. Chambers are named A, B, and C and the process flow for these six wafers (which are all of the same product type) is A-B-C. Further, assume that the required amount of processing time per wafer in each chamber is as follows: 25 seconds in A, 125 seconds in B, and 50 seconds in C. In performing a static analysis of the total time required to process all six wafers, we monitor the starting and ending time of each chamber's process for each wafer, being careful to account for possibility that blocking will occur.

Without loss of generality, assume that the six wafers to be processed are numbered from one to six. We assume the cluster tool is empty and idle, ready to begin processing wafers. Finally, we assume that a single robotic handler is present within the cluster tool and that handling time is negligible (and therefore will not be included in the analysis). Using any spreadsheet, the processing associated with wafer 1 is as displayed on the following page:

Wfr	A Start	A End	Wfr Blocked	B Start	B End	Wfr Blocked	C Start	C End	Wafer In Cass
1	0	25	0	25	150	0	150	200	200

Wafer 1 proceeds quickly through the cluster tool, completing its processing and returning back to the cassette in 200 seconds, which is the theoretical processing time associated passing through the cluster tool (i.e., 25 + 125 + 50 = 200). We continue the analysis by investigating wafer 2:

Wfr	A Start	A End	Wfr Blocked	B Start	B End	Wfr Blocked	C Start	C End	Wafer In Cass
1	0	25	0	25	150	0	150	200	200
2	25	50	100	150	275	0	275	325	325

Notice that wafer 2 is blocked for a total of 100 seconds after it completes its chamber A processing, as chamber B is the cluster tool's bottleneck chamber containing the longest required processing time. As wafer 2 cannot vacate chamber A until its destination chamber B is available, this directly impacts the time at which wafer 3 can begin its processing within the cluster tool:

Wfr	A Start	A End	Wfr Blocked	B Start	B End	Wfr Blocked	C Start	C End	Wafer In Cass
1	0	25	0	25	150	0	150	200	200
2	25	50	100	150	275	0	275	325	325
3	150	175	100	275	400	0	400	450	450

This process continues until all six wafers have completed their required processing in the cluster tool:

Wfr	A Start	A End	Wfr Blocked	B Start	B End	Wfr Blocked	C Start	C End	Wafer In Cass
1	0	25	0	25	150	0	150	200	200
2	25	50	100	150	275	0	275	325	325
3	150	175	100	275	400	0	400	450	450
4	275	300	100	400	525	0	525	575	575
5	400	425	100	525	650	0	650	700	700
6	525	550	100	650	775	0	775	825	825

In this case, all six wafers complete their processing in 825 seconds. In terms of tool performance statistics, the following quantities are readily calculated:

	Chamber A	Chamber B	Chamber C
(L1) Total Process Time	150	750	300
(L2) Total Blocked Time	500	0	0
(L3) Time Horizon	825	825	825
Chamber Processing % (L1/L3)	18.20%	90.90%	36.40%
Chamber % Blocked (L2/L3)	60.60%	0.00%	0.00%
Chamber % Empty & Idle	21.20%	9.10%	63.60%
Tool Utilization (average across all three chambers)			48.50%

The excessively large amount of time chamber A is blocked by chamber B could suggest that an additional chamber B acquisition may be needed. Again, static, spreadsheet analysis can be used to estimate the impact of adding an additional chamber B. Assuming a wafer completing its processing in chamber A can visit either chamber B1 (the original chamber B) or the new chamber B2, the static analysis associated with wafers 1 and 2 is as follows:

Wfr	A Start	A End	Blkd	B1 Start	B1 End	B2 Start	B2 End	Blkd	C Start	C End	Wafer In Cass
1	0	25	0	25	150			0	150	200	200
2	25	50	0			50	175	25	200	250	250

Again, the first wafer is processed in theoretical processing time with no queuing delays incurred. Wafer 2 experiences 25 seconds of blocking prior to entering chamber C, but completes its required processing at time = 250, 75 units earlier than in the former case wherein only one chamber of type "B" was present. The additional of the second type "B" chamber allows for the same six wafers which completed their processing at time = 825 to finish at time = 500 due to the additional of another type "B" chamber:

Wfr	A Start	A End	Blkd	B1 Start	B1 End	B2 Start	B2 End	Blkd	C Start	C End	Wafer In Cass
1	0	25	0	25	150			0	150	200	200
2	25	50	0			50	175	25	200	250	250
3	50	75	75	150	275			0	275	325	325
4	150	175	0			175	300	25	325	375	375
5	175	200	75	275	400			0	400	450	450
6	275	300	0			300	425	25	450	500	500

Again, computing cluster tool performance metrics, we find decreased block and increased tool utilization complement the 1-(500/825) = 39.4% reduction in cycle time:

	Chmbr A	Chmbr B1	Chmbr B2	Chmbr C
Total Process Time	150	375	375	300
Time Horizon	500	500	500	500
Chamber Processing %	30.00%	75.00%	75.00%	60.00%
Chamber % Blocked	30.00%	0.00%	15.00%	0.00%
Chamber % Empty & Idle	40.00%	25.00%	10.00%	40.00%
Tool Utilization				60.00%

In cases wherein processing time is widely different among the cluster tool's chambers, capacity analysis can help to properly determine the appropriate number of required chambers of each type and the resulting expected performance of the cluster tool that will result.

Dynamic, Probabilistic (Simulation) Analysis

In the previous static analysis case, all tool processing times were assuming to be fixed, constant values. In addition, the static analysis above neglected any impact of robotic handling times by assuming the time required to transfer a wafer from any chamber to

another chamber was effectively zero. While this may be an appropriate assumption for the very simple, single robotic handler tool configuration proposed above containing wafers of the same product type being loaded via a single load lock, discrete event simulation is often employed in practice when more complex cluster tool configurations are tool be evaluated, such as multiple, parallel load locks and/or dual robotic handlers. Simulation analyses are also appropriate if chamber processing times are variable, rather than fixed, deterministic values.

Simulation models generate an artificial history of the events that will take place within a fab or tool as it performs its operations. In addition to capturing the dynamics within the system or tool being modeled, such as unplanned failures and work in process (WIP) building up in queues, discrete event simulation models are capable of generating input parameter values from probability distributions. For example, if chamber A processing time were probabilistically distributed according to a Normal probability distribution with mean 25 seconds and a standard deviation of 3 seconds, a simulation model can sample from this distribution to generate actual values for chamber A processing. In this case, wafers 1-6 may have more representative processing time values of 23, 29, or 24, rather than all simply being 25 seconds.

When simulation models contain probabilistic input parameters, multiple replications or runs are required for proper analysis. However, depending on the complexity of the system being modeled, whether it is a wafer fab or a cluster tool, simulation may provide the decision maker with additional information such as a 95% confidence interval on cluster tool cycle time (i.e., a range over which cycle time will most probably vary), rather than simply a point estimate of 500 seconds, for example. The complexity of the cluster tool under study will probably drive the necessity for an appropriate modeling and analysis technique. In addition, capacity analyses can often be performed sufficiently using spreadsheet analysis, while cycle time studies often require the consideration of dynamic events and therefore, are better suited for simulation analysis. In the absence of any other modeling approaches, taking historical data and/or performing time studies is another way to estimate the cycle time required to process some quantity of wafers through a cluster tool. This sort of historical analysis can also provide insights to decision makers.

Conclusions

In this article, we have reviewed cluster tools and discussed the potential benefits and issues associated with operating cluster tools within semiconductor wafer fabs. Further, we have provided references to academic papers pertaining to advanced techniques for cluster tool capacity/throughput analysis and have presented example calculations for static, spreadsheet analysis of simple cluster tools. Finally, some discussion was provided as to why discrete event simulation is an appropriate technique for analyzing more complex cluster tools configurations containing multiple, parallel load locks and/or robotic handlers. By example, we showed the potential impact on cycle time that adding an additional chamber to a cluster tool may have, as blocking within the tool was reduced by increasing the tool's capacity. Clearly, cluster tools will continue to play a major role in fabs for some time to come. Effective capacity and cycle time analysis of cluster tools can help decision makers to understand the importance of proper configuration and operation of cluster tools.

Closing Questions for FabTime Subscribers

How do you estimate the capacity and/or cycle time of the cluster tools in your fab? Do you use static, dynamic, or some other

type of analysis methodology? If you have one, how are cluster tools modeled (i.e., at what level of detail) in your fab simulation model?

Further Reading

- Lee H.-Y., Lee T.-E., 2006, Scheduling single-armed cluster tools with reentrant wafer flows, *IEEE Transactions on Semiconductor Manufacturing,* 19(2), 226-240
- Lopez M.J., Wood S.C., 1998, Systems of multiple cluster tools: configuration and performance under perfect reliability, *IEEE Transactions on Semiconductor Manufacturing*, 11(3), 465-474
- Perkinson T.L., McLarty P.K., Gyurcsik R.S., Cavin, R.K., 1994, Single-wafer cluster tool performance: an analysis of throughput, IEEE Transactions on Semiconductor Manufacturing, 7(3), 369-373
- Rostami S., Hamidzadeh B., 2004, An optimal residency-aware scheduling technique for cluster tools with buffer module, *IEEE Transactions on Semiconductor Manufacturing*, 17(1), 68-73
- Srinivasan R.S., 1998, Modeling and performance analysis of cluster tools using Petri nets, *IEEE Transactions on Semiconductor Manufacturing*, 11(3), 394-403
- Venkatesh S., Davenport R., Foxhoven P., Nulman J., 1997, A steady-state throughput analysis of cluster tools: dual-blade versus single-blade robots, *IEEE Transactions on Semiconductor Manufacturing*, 10(4), 418-424
- Yi J., Ding S., Song D., 2005, Steady-state throughput and scheduling analysis of multi-cluster tools for semiconductor manufacturing: a decomposition approach, *Proceedings of the 2005 IEEE International Conference on Robotics and Automation*, Barcelona, Spain, 292-298
- Yim S.J., Lee D.Y., 1999, Scheduling cluster tools in wafer fabrication using candidate list and simulated annealing, *Journal of Intelligent Manufacturing*, 10, 531-540
- Zuberek W.M., 2004, Cluster tools with chamber revisiting – modeling and analysis used timed petri nets, *IEEE Transactions on Semiconductor Manufacturing*, 17(3), 333-344

Subscriber List

Total number of subscribers: 2701, from 469 companies and universities. 22 consultants.

Top 20 subscribing companies:

- Maxim Integrated Products, Inc. (216)
- Intel Corporation (158)
- Micron Technology, Inc.(89)
- ATMEL (72)
- Analog Devices (69)
- Freescale Semiconductor (66)
- Infineon Technologies (65)
- X-FAB Inc. (61)
- STMicroelectronics (60)
- Texas Instruments (56)
- Cypress Semiconductor (55)
- International Rectifier (53)
- ON Semiconductor (51)
- Chartered Semiconductor Mfg (50)
- NXP Semiconductors (50)
- TECH Semiconductor Singapore (50)
- IBM (44)
- Spansion (37)
- Seagate Technology (32)
- BAE Systems (30)

Top 3 subscribing universities:

- Virginia Tech (11)
- Ben Gurion Univ. of the Negev (7)
- Nanyang Technological University (7)

New companies and universities this month:

- California State University
- Eindhoven University of Technology
- Ismeca Semiconductor
- SEMI
- Timbercon
- Titan Ind. Ltd.
- Valience

Note: Inclusion in the subscriber profile for this newsletter indicates an interest, on the part of individual subscribers, in cycle time management. It does not imply any endorsement of FabTime or its products by any individual or his or her company.

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FabTime® Software Capacity Planning Module

Installation

For a fixed price, FabTime will:

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Do you need to answer questions like:

- Given a target product mix, do we need any new tools?
- Given the tools that we have, and the products that we are running, how many wafers can we expect to produce?
- Given our existing set of products and tools, what happens if the product mix changes? Where can we expect bottlenecks?

Are you tired of maintaining a standalone capacity planning spreadsheet?

FabTime's capacity planning module leverages the data already stored in the FabTime digital dashboard software, to make it easier to build capacity planning scenarios. The only required manual inputs are:

- Weekly ships per product.
- Product line yield percentages.

FabTime uses route information from the fab MES and calculates UPH data (tool speed) based on actual performance. FabTime also uses tool uptime performance to estimate availability (though this can be overridden). These inputs are used to generate predicted utilization percentages for each capacity type. Detailed intermediate calculations (UPH, tool productive time, tool rework percentage, etc.) are also available (an example for one tool is shown below). All outputs can be easily exported to Excel.

Capacity Planning Module Benefits

- Eliminate the need to maintain offline capacity planning models.
- Automatically update capacity planning data to reflect new conditions (process flows, tool uptime characteristics).
- Quickly run scenarios to anticipate (and avoid) bottlenecks caused by product mix changes.

C Type	Output	Value	Notes
1XStep	Rework Moves/Week	21	2004-09-06 10:00:00 to 2004-11-15 10:00:00
1XStep	Total Moves/Week	12310	2004-09-06 10:00:00 to 2004-11-15 10:00:00
1XStep	Rework Ratio	0	Rework Ratio = Rework Moves / Total Moves.
1XStep	Productive%	61	2004-09-06 10:00:00 to 2004-11-15 10:00:00
1XStep	Availability%	76.26	Availability = Productive% + Standby%.
1XStep	Historic Utilization%	79.99	Utilization (Mfg efficiency) = Productive% / Availability%.
1XStep	Productive(Rework)%	0.1	Productive(Rework)=Productive% * ReworkRatio.
1XStep	Net Availability%	76.15	Net availability% = Availability% - Productive(Rework)%.
1XStep	Arrivals (Units/Hour)	79.36	Based on total plan WGR=2025
1XStep	Tool Quantity	8	1XStep#1 ... 1XStep#8
1XStep	UPH	15.02	UPH = (TotalMoves/ToolQty) / (Productive% * 168)
1XStep	Required Hours/Day	126.84	Required hours = 24 * HourlyArrivalRate / UPH
1XStep	Predicted Utilization%	86.75	Util = 100 * ReqdHours / (24 * NetAvail * ToolQty / 100)
1XStep	Max WGR	2334.22	MaxWGR = PlanWGR / PredictedUtilization
1XStep	Historic WGR	2457.8	(Non Rework Moves) / (OperationCount / ProductCount).