FabTime Cycle Time Management Newsletter

Volume 8, No. 8 September 2007

Information

Mission: To discuss issues relating to proactive wafer fab cycle time management

Publisher: FabTime Inc. FabTime sells cycle time management software for wafer fab managers. New features in this month include a ToTool functionality on Forecast Outs Charts (to predict which lots will be arriving at a particular tool during a given future time window).

Editor: Jennifer Robinson

Contributors: Ulrich Dierks and Thomas Quarg (AMD); Professor Scott Mason (University of Arkansas)

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Welcome

Welcome to Volume 8, Number 8 of the FabTime Cycle Time Management Newsletter! We hope that the fall season is finding you all well. This month we have community announcements about a FabTime demo offer, and some upcoming industry meetings that I'll be attending. If you'll be attending, too, I'd love to have the chance to meet you. Our FabTime software tip of the month is about using FabTime to predict when lots will complete processing in the fab. We also have some subscriber discussion regarding batch tools, a continuation of an earlier topic introduced by Walt Trybula.

In our main article this month, written by Professor Scott Mason, we discuss the impact that the way lots are released into a wafer fab can have on performance. We provide an overview of workload (flow) control terminology, and then briefly discuss both push- and pull-based methods. Finally, after discussing recent results from case studies, we conclude by returning to last month's newsletter topic, dispatching in wafer fabs, to discuss advanced dispatching strategies for linked process steps. We conclude with three recommendations for evaluating lot release policies used in fabs. We hope that you find this article useful.

Thanks for reading!—Jennifer

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Community News/Announcements

FabTime Demo Offer

We've heard some feedback recently about FabTime's software, along the lines of "Wow, this is much more powerful than I expected" and "I wish I had FabTime five years ago". We were inspired to mention this to you, our newsletter subscribers, because we think it's likely that some of you would be interested in the product if you knew more about it. And of course the best way to learn more about a product is not to hear marketing-speak, but to see it in action. So, if you work in a wafer fab, and you'd like to arrange for a quick FabTime demonstration, please contact sales@FabTime.com, and we'll be more than happy to set something up. We may be able to visit your site (especially for fabs in the US), or we can arrange to do a demo with you via the Internet.

Upcoming Industry Meetings

FabTime's Jennifer Robinson will be attending the Fab Owners Association meeting in Temecula, CA on October 17th and 18th (details here: waferfabs.org/-calendar.html), and will probably be at the 4th ISMI Symposium on Manufacturing Effectiveness in Austin the following week (details here: ismi.sematech.org/-ismisymposium/). If you will be attending either of these meetings, and would like to arrange to meet Jennifer, you can email her at Jennifer.Robinson@FabTime.com.

FabTime welcomes the opportunity to publish community announcements. Send them to newsletter@FabTime.com.

FabTime User Tip of the Month

Predict When Individual Lots Will Complete Processing

Did you know that FabTime can show you predicted completion dates for your lots? For individual lots, the chart to use for this is the Lot Progress chart. You can access this chart in three ways:

1. From the Charts page, click "Show" next to "Lot Charts", and then click "Go" next to "Lot Progress Chart". You'll be prompted to enter a Lot ID in the "Lot:" filter. Enter the Lot ID and press Enter, or click the "Go" button, to generate the Lot Progress chart.

2. From any chart that lists individual lots (e.g. the WIP Lot List chart or the Moves Lot List chart), click on the gray "Progress" link beneath that Lot ID in the data table. This takes you directly to the Lot Progress chart for that lot.

3. From the Lot History chart for a particular lot, use the "Quick Jump" drop-down above the data table to switch to the Lot Progress chart. This is the only chart you can jump to from the Lot History chart (and vice versa).

What the Lot Progress chart shows is both past and future operations, with a column for each step. The height of each column corresponds to the completion date for that step (shown on the y-axis). Steps that have already been completed will be

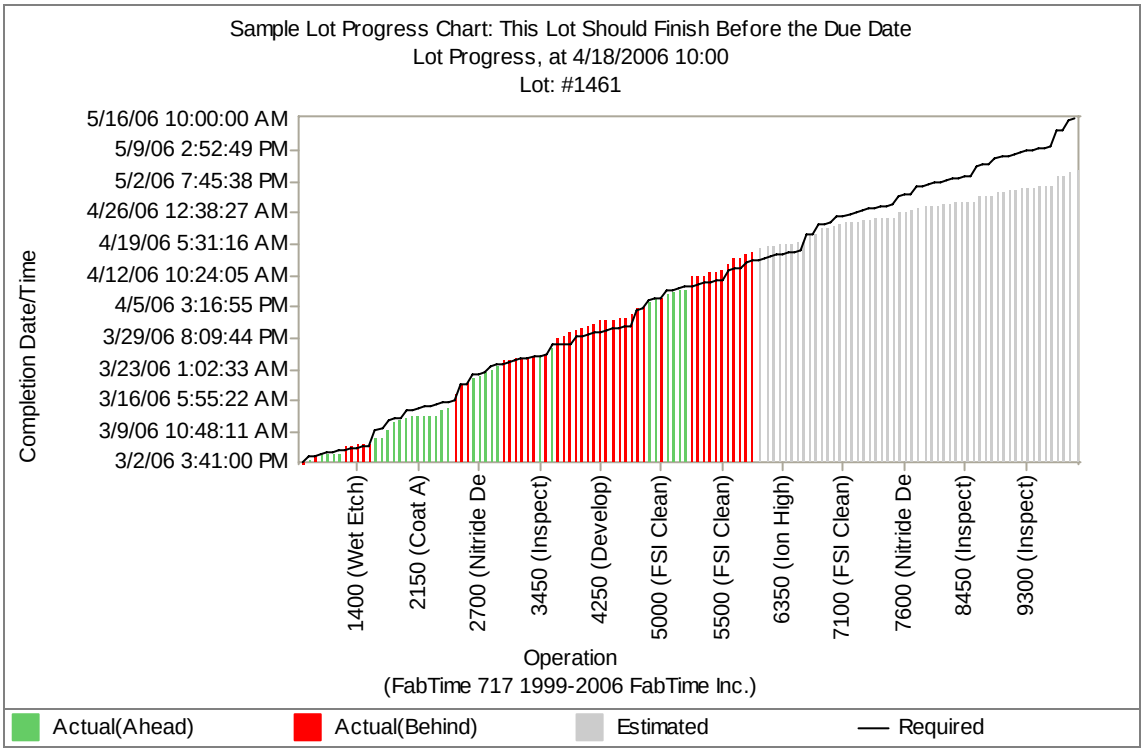
displayed as red or green, depending on whether the lot was ahead of or behind schedule at that step. Future steps will be displayed as gray columns. The y-axis value corresponding to the right-most column represents the expected lot completion date, based on the planned cycle time values stored in FabTime for each step. The y-axis value corresponding to the right-most point on the solid black line represents the lot's due date. The other points on the black line show where the lot should be at each step, in order to reach the due date (scaled based on planned cycle times at each step). If the last gray column is higher than the black line, then the lot is projected to be late, given the expected cycle time of future steps. An example of a lot that is not projected to be late is shown below.

You can do some limited what-if analysis with this chart, by using the "Xfctr:" filter. This filter influences what x-factor (multiple of theoretical cycle time) is used to generate the estimates for planned cycle times by step. Entering a "2", for example, will cause FabTime to show you the expected shipment date that would be achieved if all of the future steps were completed in twice the theoretical cycle time. This is a quick way to look at what you might achieve by making the lot hot, for example.

The Lot Progress chart relies on these estimates for cycle time at future steps, and does not currently take fab status into account. Therefore, it will only be as accurate as the quality of your planned cycle time data. If you don't yet have planned cycle time data in your FabTime database (e.g. you don't get any gray columns on the Lot Progress chart), please contact us. We'll be happy to work with you to extract this from your MES, or to estimate it for you using historical data.

You can also use FabTime to generate a list of lots that are expected to be completed within some time period. This is done using the Forecast Outs Lot List chart, described in a previous tip.

If you have any questions about this feature (or any other software-related issues), just use the Feedback form in the software.



Subscriber Discussion Forum

Batch Tool Capacity

Ulrich Dierks and **Thomas Quarg** (both from AMD in Dresden) submitted comments (and a spreadsheet example) in response to the previous subscriber discussion topic regarding capacity and loading policy on batch tools. Ulrich wrote: "We would like to participate in the BatchTool capacity discussion. "If you hold a batch tool idle as to run with a full batch might this make it a bottleneck?". Attached an EXCEL model of two identical configurable batch tools, with configurable loading (press F9, or change "feed wfr" in Column C). One tool (called Partial Batch) runs batch after batch without waiting as long as any material is available. The other one (called Full Batch) waits until a full batch is available. The model contains 600 hrs of infinite running for both tools. In my humble opinion, there would have been no difference in result if both tools would have had identical downtime periods during the experiment.

Results: A batch tool will hardly become a bottleneck by waiting for full batch, if it is not a bottleneck anyway. For the batch tool itself there is no significant capacity impact to wait for a full batch. For the single recipe tool in the model the worst case impact is one batch of wafers waiting behind a tool run with partial batches during an ideally infinite period. There are even cases that supply slightly more throughput in case of waiting for complete batches, e.g. when needed lots arrive shortly after a partial batch start. The more different recipes need to be supported the more capacity loss by waiting might occur, but worst case is one run's load per performed recipe. Waiting for full batch is always best for the batch tool's production cost, but can be suboptimal for downstream bottlenecks (due to starving) and is always bad for cycle time and variance of service rate.

Conclusion: The struggle is not primarily: Cost vs. capacity, but cost vs. cycle time and variance. The impact gets smaller with increase in the tool's load size.

Potential Solution: Optimized batch loading by dispatch rules will improve cycle time and variance & will lead to cost improvement versus simple partial strategy. Dispatch strategy may be: Waiting to complete a 4 lot batch: <25% of PT for last lot, <50% for 2 remaining lots using "look ahead" algorithms and if lots will not arrive in specified window, just run with batch on hand."

Thomas Quarg added: "In addition to Ulrich's contribution I would like to use the opportunity to express my estimation for your latest edition of FabTime Newsletter, it's interesting as usual, and to refer to information on my team's solutions to overcome THP problems by dispatching and loading strategies. At the upcoming MASM Conference (IEEE - Scottsdale, Arizona, USA - September 22-25, 2007 - www.fulton.asu.edu-/~case2007/index.php) Kilian Schmidt, member of our Industrial Engineering Team, will present a paper on "Improving dispatch rules for cascading tools". This gives an idea of how this kind of problems can be solved. An abstract follows.

Improving dispatch rules for cascading tools

Gero Grau, Jörg Weigang, Kilian Schmidt

Abstract— Line balance and tool throughput are two important, yet conflicting goals. Especially for cascading tools supporting multiple layers in the line, there has to be a trade off between these two optimization criteria. Short cascades are optimal for line balancing, but this strategy leads to lower tool throughput. The size of the negative throughput impact is even stronger when tools require setup times for the switch from one cascade performing recipe A to another cascade

performing recipe B. In the semiconductor industry, state-of-the-art dispatch rules are widely used as a tool to calculate optimal operational decisions. The paper presents an approach on how to combine the two criteria in a dispatch rule."

FabTime Response:
We appreciate Ulrich and Thomas for taking the time to address this question, and for sending us such a nice spreadsheet tool for examining these issues. We agree with Ulrich's conclusions, particularly regarding the cycle time increase from waiting for full batches, and we look forward to reading the paper that Thomas mentioned. If any subscribers would like to see a copy of Ulrich's spreadsheet model, email your request to newsletter-@fabtime.com.

Wafer Fab Flow Control via Order Release

Introduction

People who run fabs are always looking for ways to control WIP and to meet both cycle time and throughput-based targets. In this article, we discuss the impact that the way lots are released into the fab can have on performance. Below, we provide an overview of workload (flow) control terminology, and then briefly discuss both push- and pull-based methods. Finally, after discussing recent results from case studies, we conclude by returning to last month's newsletter topic, dispatching in wafer fabs, to discuss advanced dispatching strategies for linked process steps.

Background

Workload (or flow) control is defined as the combination of lot (order) release and dispatching strategies used to control the flow of lots through a wafer fab. While earlier literature suggests that order release methods may be the most important aspect of flow control, even to the point of being more important than dispatching, today's fabs often focus on due-date related delivery performance. When due dates are important, simple first-in, first out dispatching strategies are often ineffective (in fact, this motivates the wide usage of critical-ratio type dispatching rules as discussed in last month's newsletter). Order (lot) release is the point at which a lot moves from the production planning domain to the shop floor control domain.

Push-based order release philosophies simply release all lots for which material and process flows are available. This approach is based on the hope that what one puts into the fab is what one will get out of the fab, with little recognition of capacity or congestion issues. Without proper understanding of a fab's underlying capacity capability, large WIP levels and high cycle times can result under pure push approaches.

In order to make "smarter" starts, some fabs choose to constrain the total WIP present in the fab, only starting lots once some equivalent number of wafers has completed processing. This approach, CONWIP (Spearman et al. 1990), focuses on WIP control, rather than throughput control and is a generalization of Kanban in that the number of Kanban cards equals the desired number of wafers in WIP.

Order release strategies based on pull concepts began to emerge after the appearance of Japanese management concepts like Just-in-Time (JIT) and Kanban cards. While push approaches are driven by what one desires to produce, pull approaches are driven by what one is capable of producing. At the same time interest in JIT and Kanban was accelerating, bottleneck scheduling philosophies developed a strong following. These revolved around identification of bottleneck processes and using bottlenecks as a central focus of control strategies. Goldratt and Fox's The Race (1986) provides a motivational and conceptual view of the authors' "drum-buffer-rope" approach to production control.

The idea is that the slowest paced (bottleneck) process provides the pace (drum). This is tied to the system entry points (ropes), and the bottleneck is always provided with a time-phased inventory of work (buffer) that guards it from being idle or starved. Unfortunately, very few case studies have documented the successful deployment of drum-buffer-rope in wafer fabs. The long, re-entrant process flows and unreliable nature of semiconductor manufacturing equipment tend to make drum-buffer-rope and Kanban-type approaches fail in application. Tyan et al. (2002) developed a fab state-dependent dispatching rule that considered cycle time, WIP, throughput, and due date delivery performance. However the impact of such a rule is unproven because the rule was only tested on a "near-real-world" fab model, not in an actual fab environment.

Semiconductor Manufacturing Workload Control

Some wafer fabs start new wafer lots in quantities equal to the maximum batch size of the first batch processing step (e.g., initial oxidation; if the fab has 25 wafer lots and the oven can handle four lots, start four lots of new wafers at a time). While this approach can indeed provide excellent batch utilization early in the process flow, proper analyses should be performed via capacity models and/or simulation to confirm that the fab's bottleneck toolgroup can accommodate this number of wafer starts over time. One potential unintended consequence of this type of lot release plan is when the toolgroup directly after the early diffusion step inadvertently becomes the fab's bottleneck. This can occur when the toolgroup after the diffusion step is already operating at or near capacity prior to the implementation of this multiple lot starts release plan. This suggests the necessity for proper analysis prior to deployment of proposed order release strategies, as order release to the fab can play a significant role in determining product cycle times (Sivakumar et al., 2001).

The majority of recent published literature in wafer fab workload control focuses on line balancing and the consideration of capacity constraints. Specifically, researchers have worked towards maintaining comparable amounts of required processing or cycle time in front of tools and/or segments of the process flow. Chen et al. (2002) develop production plans by blending line balance, on-time delivery, and bottleneck utilization factors in a real world fab. Maintaining appropriate WIP levels throughout the fab can be accomplished both through effective order release and smart dispatching decisions. The fab associated with the Chen et al. (2002) study realized on-time product delivery and appropriate bottleneck loading levels with little to no starvation issues after deploying their multi-criteria production planning methodology.

Chung et al. (2003) develop an approach to plan lot release into a fab by first establishing batch loading factors/policies, and then calculating system control parameters like WIP levels and planned bottleneck operations (moves). The plan uses desired process step cycle times and

tool throughput rates as inputs. Finally, a CONWIP-like approach is combined with prior calculations to establish the associated order release plans. In addition, wafer starts and target WIP levels are used to determine the resulting throughput expectation of the fab, which in turn can be used to plan acceptable customer due dates for lots.

While this previous work of Chung et al. (2003) used a mathematical modeled-based strategy, Hu et al. (2003) make some initial simplifying assumptions to perform a queuing analysis of a fab. They derive flow control parameters in terms of both the mean and variability associated with the input process for each fab toolgroup. Using this knowledge, the authors compute realistic, obtainable performance targets for process step cycle times and WIP levels. However, though simulation experimentation supports the assertion that the authors' approach is viable for real world implementation, no additional published work shows that it has in fact been put into practice. Purely speculating, it would seem that queuing network-based approaches, while academically interesting, are far less accepted by industry fab personnel.

In an attempt to tie together front end wafer fabrication with back end assembly/packaging/test operations, Pai et al. (2004) investigate methods for achieving planned back end shipment targets through effective order release and dispatching decisions in the front end of their fab. The authors' approach involves comparing current fab WIP to target levels, and then prioritizing or de-prioritizing WIP according to its intended destination and the amount of work already there. Considering both front and back end operations in concert, the authors demonstrate through a simulation study that while line balance is not fully achieved according to desired specification, back end shipment goals are met using this coordinated, capacitated strategy.

In terms of the backend of semiconductor manufacturing, Chua et al. (2007) present a capacitated lot release system that functions in a highly constrained, high product mix environment. Lots are prioritized according to various factors, including capacity constraint relationships that impact what the lot will experience according to its corresponding process flow. As available capacity is identified and allocated to lots waiting to be started, the system reportedly adapts to changing manufacturing environment conditions automatically. As less capacity is available, the system in turn "throttles down" the number of lots started into the factory. Therefore, this order release strategy is able to effectively comprehend the factory's current capacity limitations and translate this information into capacity-feasible lot release plans.

Dispatching Linked Process Steps

On some occasions, once effective fab order release policies are tested and in place, it is desirable to control the behavior of a group of process steps via advanced dispatching. For example, consider the case when a cleaning tool performs some type of pre-clean step prior to feeding a downstream processing tool. Often, a cleaned wafer or lot is required to begin processing on the downstream tool within some pre-specified amount of time (e.g., four hours); otherwise, if cleaned wafers/lots do not begin their downstream processing within the allowable timer limit, they must be re-cleaned prior to subsequent processing. This phenomenon is known as a time bound sequence (among other names). Proper dispatching within this group of process steps is a necessity to avoid unwanted, costly reworking (re-cleaning) of lots.

In practice, the fab operator running the clean tool often communicates with the downstream tool operator (or vice versa) to establish when the downstream tool will be once again ready to accept another lot

(or group of lots in the case when the downstream tool is a batch tool). However, depending on the size and complexity of the fab, it is not uncommon for multiple different tools or processes to exist downstream from the cleaning tool. This added complexity can make communication difficult between the different types of operators involved. Also, the effectiveness of operator communications often varies across shifts and/or areas of the fab.

Further, consider the case when the cleaning tool itself is a batch tool. If the clean tool can process more lots than a tool that it feeds downstream, a time bound sequence or "timer" value could be violated if more lots are sent downstream than can be processed within the allowable timer length. For example, if a clean tool can process six lots of wafers, but the downstream deposition tool is a single lot tool, the timer length must be at least equal to six times the downstream tool's single lot processing time, not to mention accounting for travel time, tool load/setup/unload times, and operator interactions. Therefore, if the downstream tool requires 45 minutes per lot and the maximum timer length is three hours, only in a perfect (albeit non-realistic) case could four lots be processed on the upstream tool. Almost certainly, material handling and/or processing delays will cause at least one of the lots to be reworked.

With these factors in mind, it may be prudent to stage all WIP in front of the cleaning tool, rather than having any lots waiting in front of the linked, downstream tools. In this way, dispatching decisions can be made upstream at the cleaning tool based on the estimated time that pertinent downstream tools will become available to accept subsequent lots for processing. In this way, proper care can be taken to ensure what gets processed upstream is in no way in jeopardy of violating timer lengths, even in the case when the maximum batch size of the upstream tool does not perfectly match the batch size capacity of the downstream tool(s). FabTime's NextStep rule considers these factors when forming appropriate batches on both up- and downstream tools.

However, care must be taken to ensure the some mechanism or process is in place to notify both fab operators and the fab's MES/dispatching system of any planned lot "reservations" across a linked group of tools. For example, consider the case when a group of lots are selected for cleaning with the intent of being sent immediately to their next required processing step in order to satisfy a timer requirement. In this case, the downstream tool must be "reserved" for these lots being cleaned so that someone else at another fab terminal does not mistakenly load some other lots onto it. In addition, the lots being cleaned must be labeled or marked as already assigned to the downstream tool so that they are not mistakenly assigned to a different tool.

Therefore, under this type of reservation scheme, there may be some amount of time the downstream tool is held idle, waiting for the clean lots to arrive in order to ensure time bound sequences are followed. Similarly, in the event the previously reserved downstream tool fails or otherwise is unable to process the intended set of clean lots, the currently marked (reserved), clean lots must be allowed or forced to return to the general pool of lots in queue after some amount of time. In other words, both downstream tool and lot reservations are temporal in that they are important to promoting effective linked step dispatching, but also must "reset" themselves for subsequent reassignment should some unexpected event occur with respect to either the up or downstream linked tools. This is how the NextStep rule in FabTime's dispatching module functions.

In fact, the type of linked-step dispatching described above does not necessarily need to occur only between two adjacent

processing steps. It may be desirable to maintain some amount or target level of WIP within the block of processing steps, like in the case where the last downstream step in the block is performed by a photolithography stepper or other fab bottleneck tool. The spirit of this type of rule functionality is to help avoid starving critical tools of WIP (i.e., keeping bottleneck tools fed properly, allowing them to process wafers).

Conclusions

The primary takeaway from this discussion of wafer fab flow control is that any lot release approach a fab manager wishes to employ should be evaluated in terms of 1) capacity feasibility, 2) impact on tools that are at or near capacity and are not intended to be fab bottlenecks, and 3) bottleneck tool loading/starvation considerations. Factory dynamics can and do react differently to releasing the same total number of wafers in different quantities over different periodic intervals (e.g., 100 wafers every two hours vs. 50 wafers every hour). While regularly increasing fab input rates (and therefore WIP) can help ensure that bottleneck tools never starve, careful analyses may show that reducing start rate levels can help to promote a more balanced, efficient production line wherein WIP is queued at expected locations and expected bottleneck resources are indeed the limiting resources in the fab.

Closing Questions for FabTime Subscribers

How is lot/order release performed in your fab (constant rate, bursts of multiple lots periodically to match first batch processing step's batch size, other smoothed or periodic approaches)? What steps do you take to make sure your bottleneck production equipment always has lots/WIP in front of it? Is this accomplished through capacitated production planning, dispatching strategies, or other methods?

Further Reading

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- Chua, T.-J., Liu, M.-W., Wang, F.-Y., Yan, W.-J., Cai, T.-X., 2007, "An intelligent multi-constraint finite capacity-based lot release system for semiconductor backend assembly environment," *Robotics and Computer-Integrated Manufacturing*, 23 (3), 326-338.

- Chung, S. H., Pearn, W. L., Lee, A. H. I., and Ke, W. T., 2003, "Job Order Releasing And Throughput Planning For Multi-Priority Orders In Wafer Fabs," *International Journal of Production Research*, 41 (8), 1765-1784.

- Hu, M. D., Chang, S. C., 2003, "Translating Overall Production Goals into Distributed Flow Control Parameters for Semiconductor Manufacturing," *Journal of Manufacturing Systems*, 22 (1), 46-63

- Pai, P. F., Lee, C. E., and Su, T. H., 2004, "A Daily Production Model for Wafer Fabrication," *International Journal of Advanced Manufacturing Technology*, 58-63.

- Sivakumar, A. I., Choong, N. F., Chong, C. S., 2001, "Modeling causes and effects of semiconductor backend cycle time," *Solid State Technology*, 44 (12), 51-55.

- Spearman, M. L., Woodruff, D. L., and Hopp, W. J., 1990, "CONWIP: a pull alternative to kanban," *International Journal of Production Research,* 28(5), 879-894.

- Tyan, J. C., Chen, J. C., and Wang, F. K., 2002, "Development of a State-Dependent Dispatch Rule using Theory of Constraints in Near-Real-World Wafer Fabrication," *Production Planning & Control*, Vol. 13, No. 3, 253-261.

Subscriber List

Total number of subscribers: 2757, from 417 companies and universities. 22 consultants.

Top 20 subscribing companies:

- Maxim Integrated Products, Inc. (253)
- Intel Corporation (160)
- Micron Technology, Inc. (87)
- ATMEL (71)
- Analog Devices (67)
- Infineon Technologies (67)
- Freescale Semiconductor (65)
- X-FAB Inc. (59)
- Texas Instruments (56)
- STMicroelectronics (55)
- Cypress Semiconductor (54)
- International Rectifier (52)
- ON Semiconductor (51)
- TECH Semiconductor Singapore (51)
- Chartered Semiconductor Mfg (50)
- NXP Semiconductors (49)
- IBM (45)
- Spansion (38)
- Seagate Technology (32)
- BAE Systems (30)
- Maxim Integrated Prod., Inc. (252)

Top 3 subscribing universities:

- Virginia Tech (11)
- Ben Gurion Univ. of the Negev (7)
- Nanyang Technological University (7)

New companies and universities this month:

- Mazik Media
- MTS Systems
- Rochester Institute of Technology
- SSCM Consulting
- Solyndra
- Stryker (Medical Device Co.)
- SVTC
- TESCO HSC

Note: Inclusion in the subscriber profile for this newsletter indicates an interest, on the part of individual subscribers, in cycle time management. It does not imply any endorsement of FabTime or its products by any individual or his or her company.

There is no charge to subscribe and receive the current issue of the newsletter each month. Past issues of the newsletter are currently only available to customers of FabTime's web-based digital dashboard software or cycle time management course.

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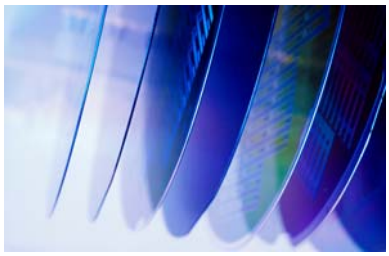
FabTime® Dispatching Module



Dispatch Configuration

Configuration projects are quoted on a fixed price basis for each site, and typically include:

- Dispatch rule and factor configuration.
- Training.
- Dispatch list feed to the MES (if applicable).

Dispatch Factors

- Batch code at the current tool.
- Lot priority.
- Downstream tool priority.
- Current tool FIFO.
- Current tool idle time.
- Downstream batch efficiency.
- Critical ratio.
- Earliest-due-date.
- Current step processing time.
- Remaining processing time.
- Current step qualified tool count
- WIP level at downstream tools.
- Up to five other site-specific factors.

Interested?

Contact FabTime for technical details.

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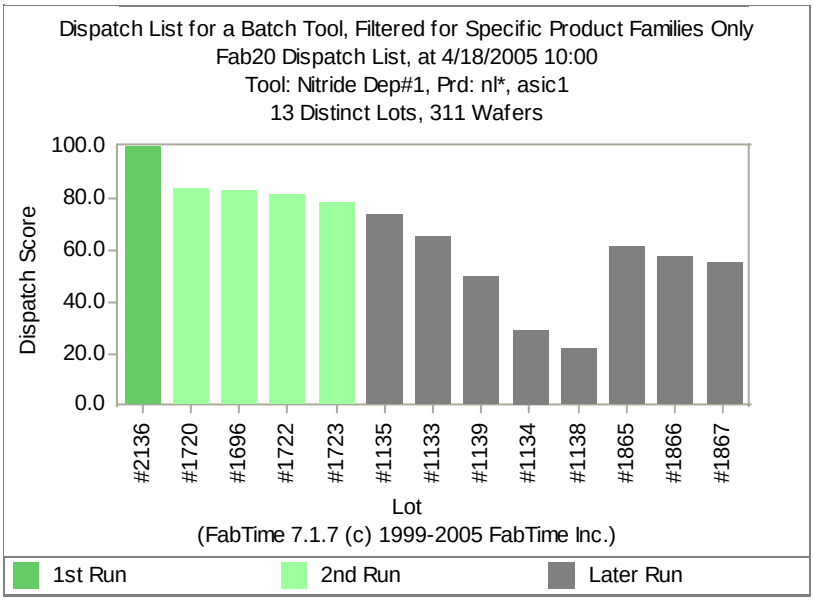
Web: www.FabTime.com

Do your operators make the best possible dispatching decisions?

- Do you struggle to balance lot priorities and due dates with tool utilization and moves goals?
- Do your critical bottleneck tools ever starve?
- Do you use standard dispatch rules, but feel that your fab's situation is more complex, requiring custom blended rules?
- Do you know how well your fab executes your dispatching?

FabTime's dispatching module is an add-on to our **web-based digital dashboard software**. At any point, for any tool in your fab, FabTime will show you the list of all lots qualified to run on that tool. This list will be ordered by the dispatching logic that your site has selected for that tool. This logic can use standard dispatch rules such as Priority-FIFO and Critical Ratio. However, you can also create custom dispatching logic using any combination of dispatch factors (shown to the left).

You can display dispatch lists in FabTime, and/or export them back to your MES. FabTime also includes a dispatch reservation system to hold downstream tools when a lot is started on an upstream tool, as well as dispatch performance reporting.



FabTime Dispatching Module Benefits

- Ensure that wafers needed by management are in fact the wafers that are run, while requiring less manual intervention on the part of management.
- Improve delivery to schedule, and the display of performance to schedule.
- Document the dispatching logic used by the best operators and make this available to all shifts.